

HAWAA

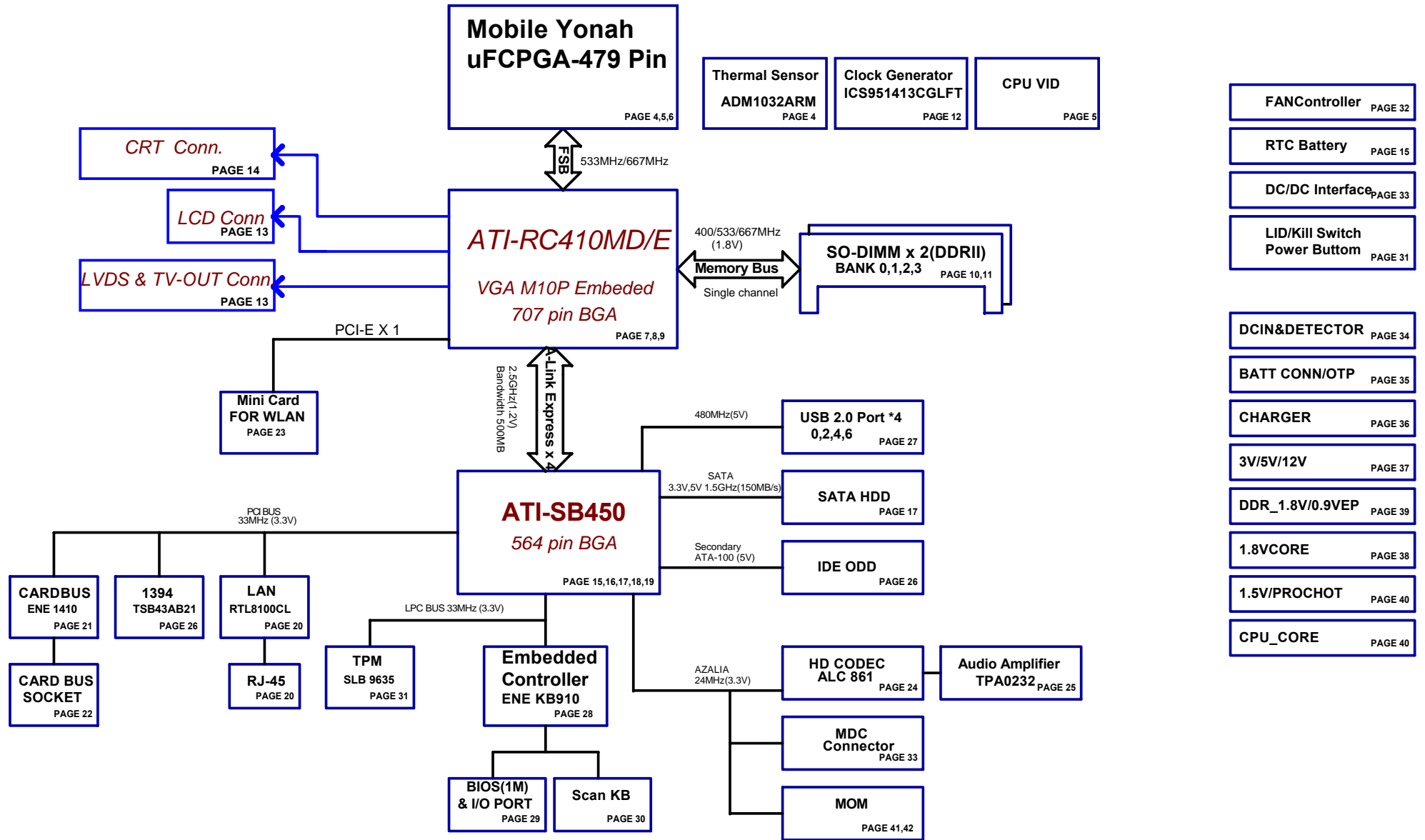
LA-3141 REV 0.3 Schematic

uFCPGA Yonah/ ATi-RC410MD(A12)/ ATi-SB450(A13)
2006-01-26 Rev.0.3

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2005/11/01	Deciphered Date	2006/11/30	Title	Black Diagram
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hexrain@hotmail.com

HAWAA LA-3141 FUNCTION BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.2VS	1.2VS for PCI-Express	ON	OFF	OFF
+0.9VS	0.9V switched power rail	ON	OFF	OFF
+1.5VS	Yonah	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8V	1.8V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#GNT#	Interrupts
ENE 1410	AD20	2	PIRQB
LAN	AD22	1	PIRQG
1394	AD16	0	PIRQA

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b

EC SM Bus2 address

SB450 SM Bus address

Device	Address
Clock Generator (ICS951413BGLFT)	1101 001Xb
DDRII DIMM0	1010 0100b A4
DDRII DIMM1	1010 0110b A6

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc	100K +/- 5%			
Board ID	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

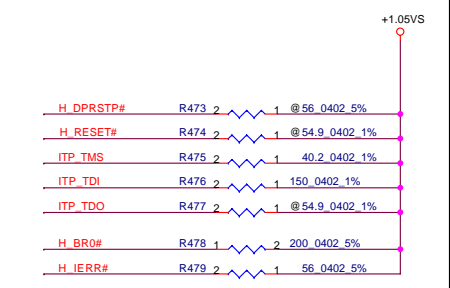
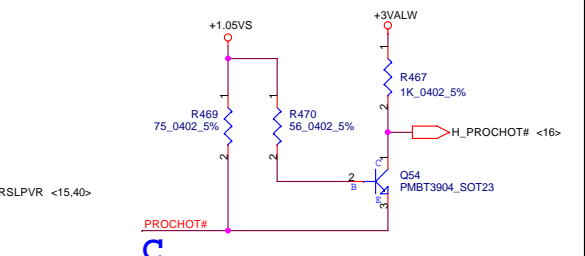
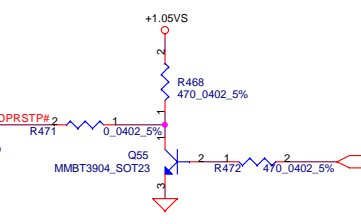
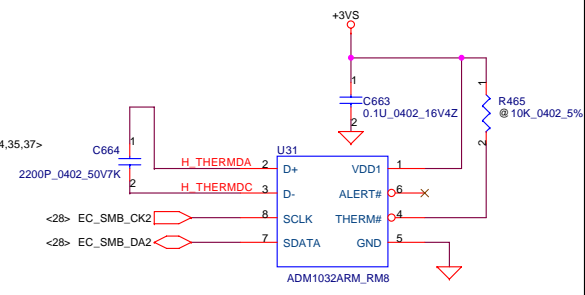
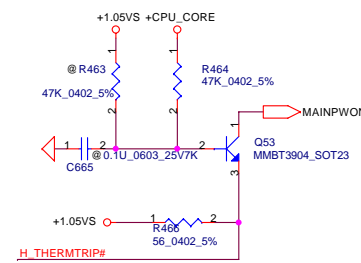
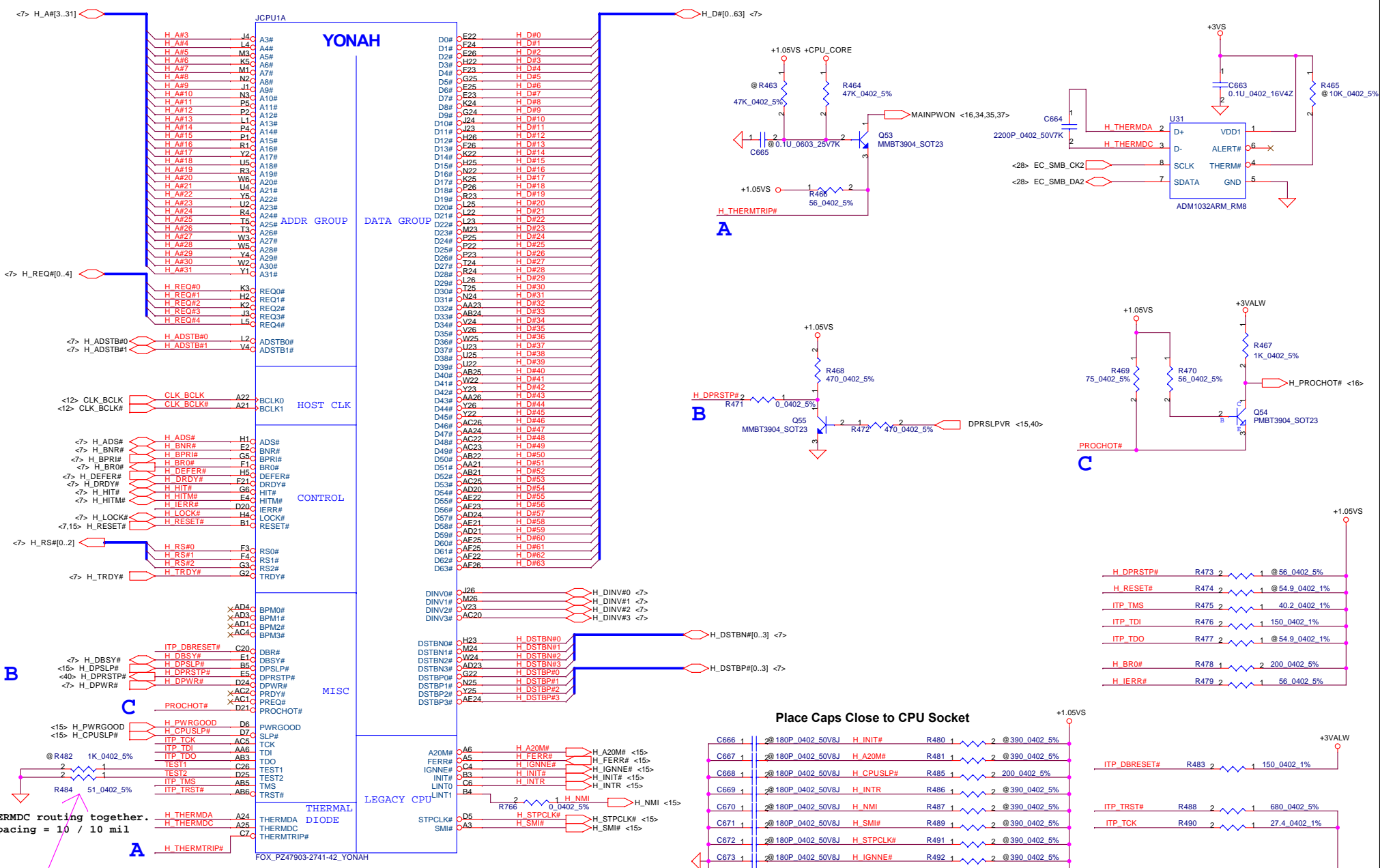
SKU ID	PCB Revision
0	-
1	SKU 1
2	SKU 2
3	SKU 3
4	SKU 4(JP)
5	SKU 5
6	
7	

BTN ID	BTN Status
0	1 Buttons
1	
2	
3	
4	6 Buttons
5	
6	
7	

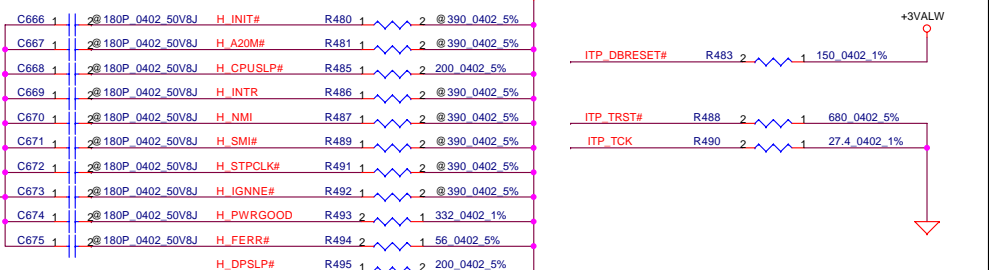
BTO Function	BOM structure
1394	1394@
Wireless LAN	WLAN@
TV-OUT	TVOUT@
TPM	TPM@

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Place Caps Close to CPU Socket

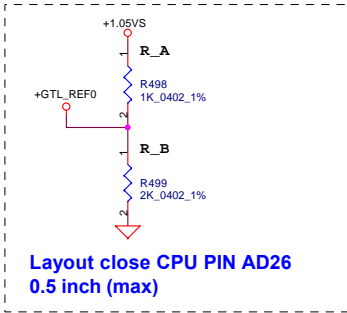
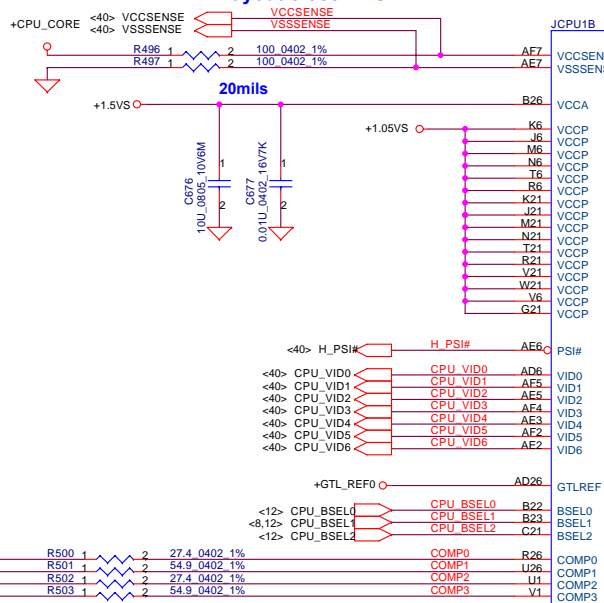


H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil

For B-0 stepping engineering samples (ES) of Celeron M processor need to pop this 51 ohm resistor.

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**Length match within 25 mils
Layout close CPU**



**Layout close CPU PIN AD26
0.5 inch (max)**

CPU_BSEL	CPU_BSEL0	CPU_BSEL1	CPU_BSEL2
133	0	0	1
166	0	1	1

TRACE CLOSELY CPU < 0.5"

COMP0, COMP2 layout : Width 18mils and Space 25mils
COMP1, COMP3 layout : Space 25mils

YONAH

YONAH

POWER, GROUND, RESERVED SIGNALS AND NC

POWER, GROUND

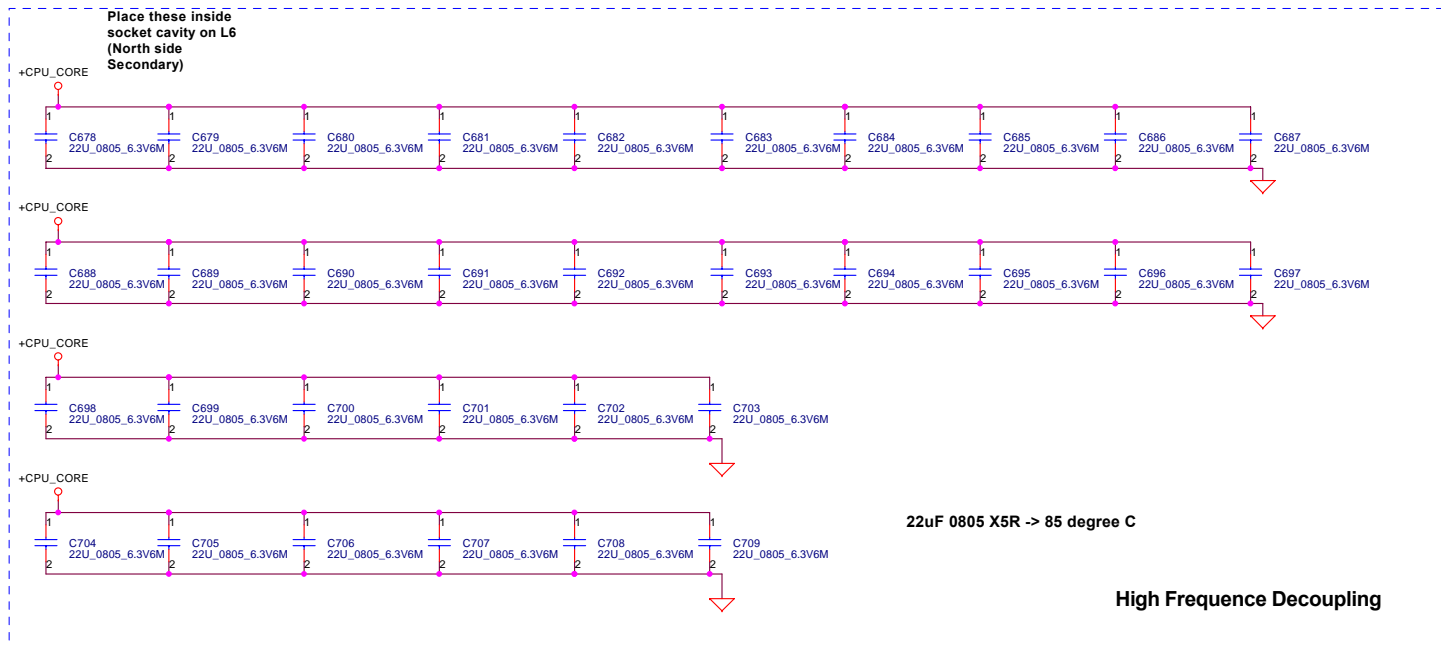
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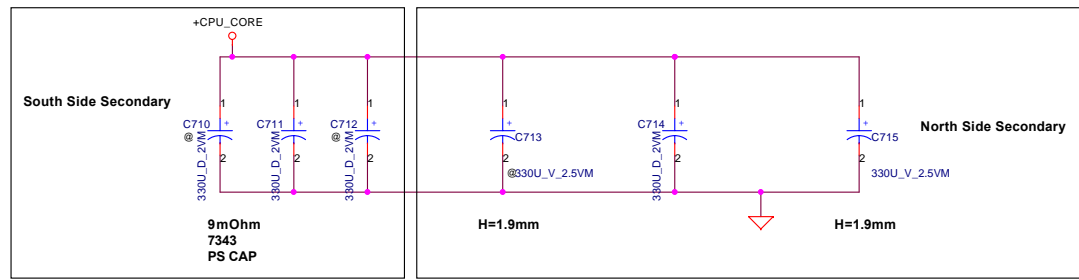
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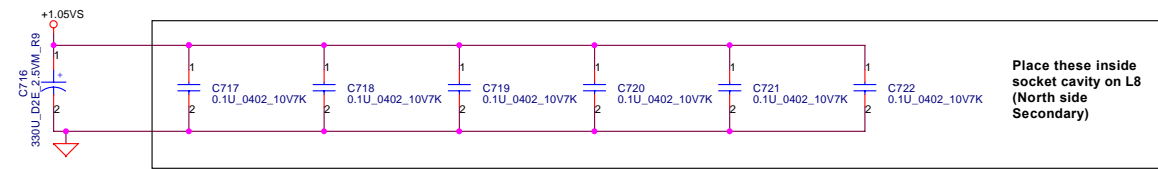
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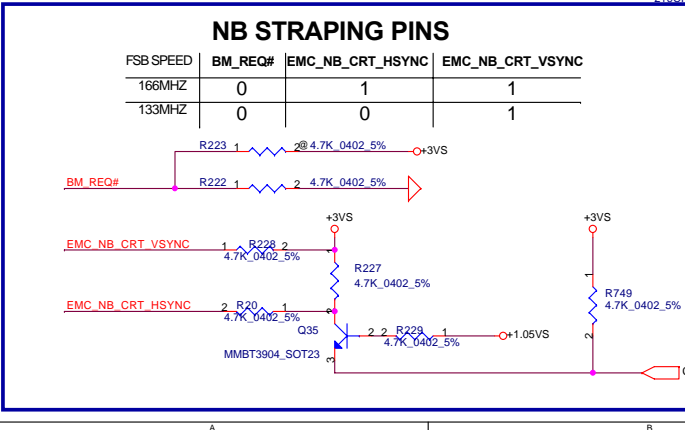
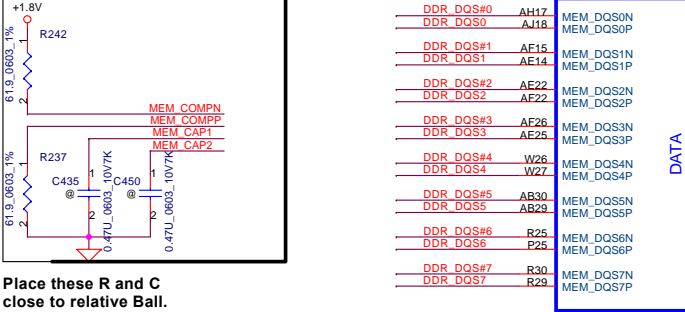
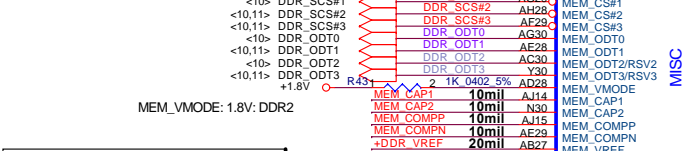
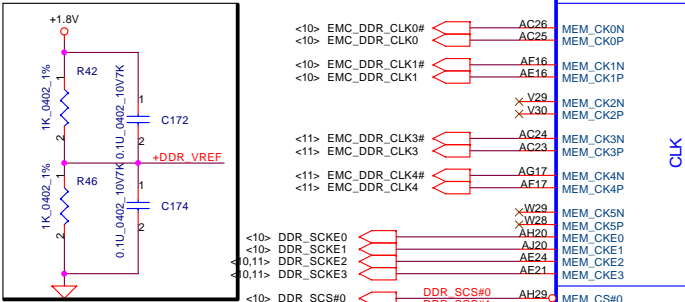
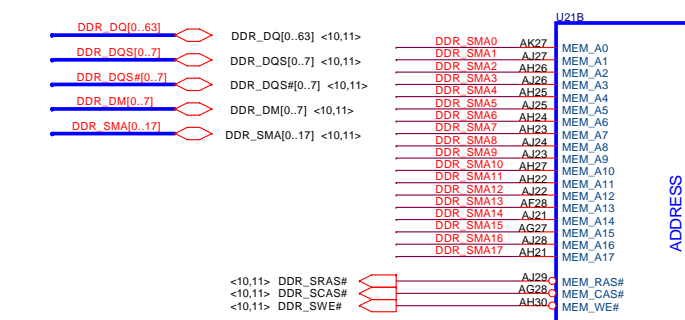
Near VCORE regulator.



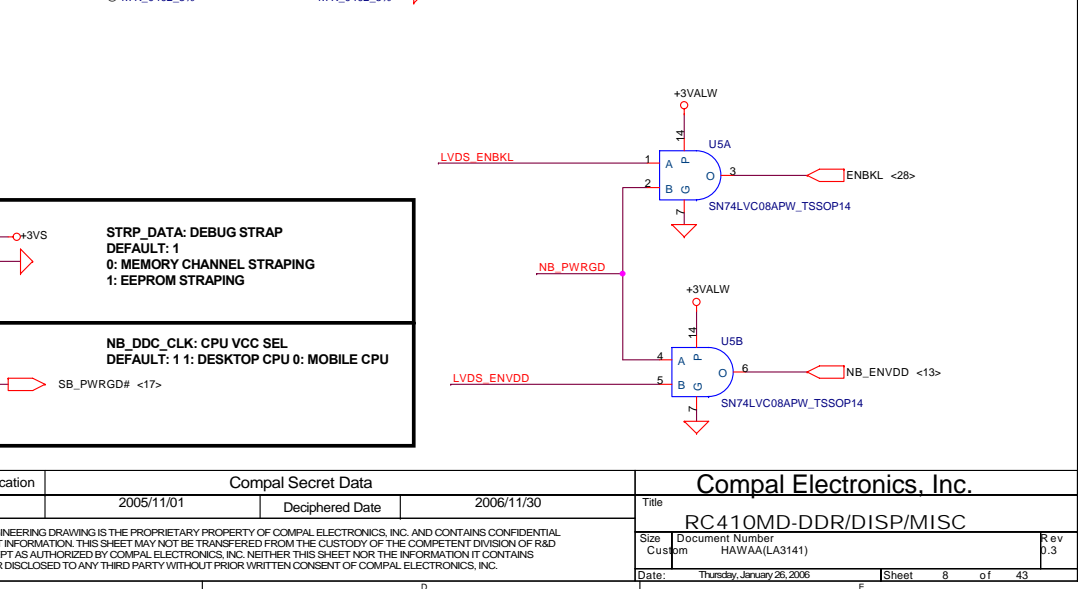
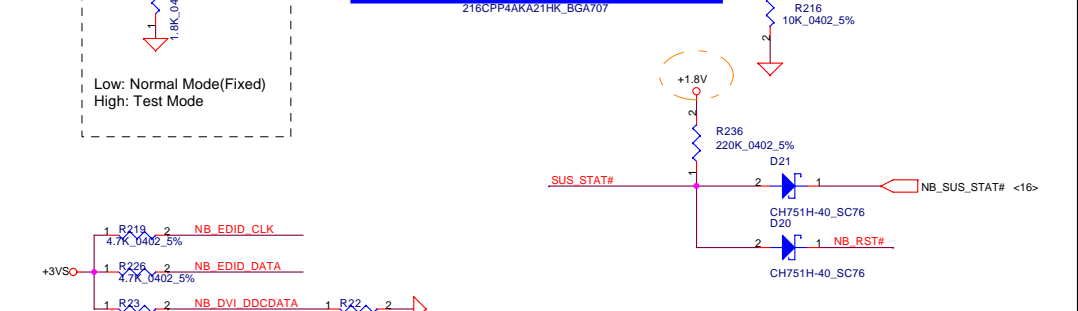
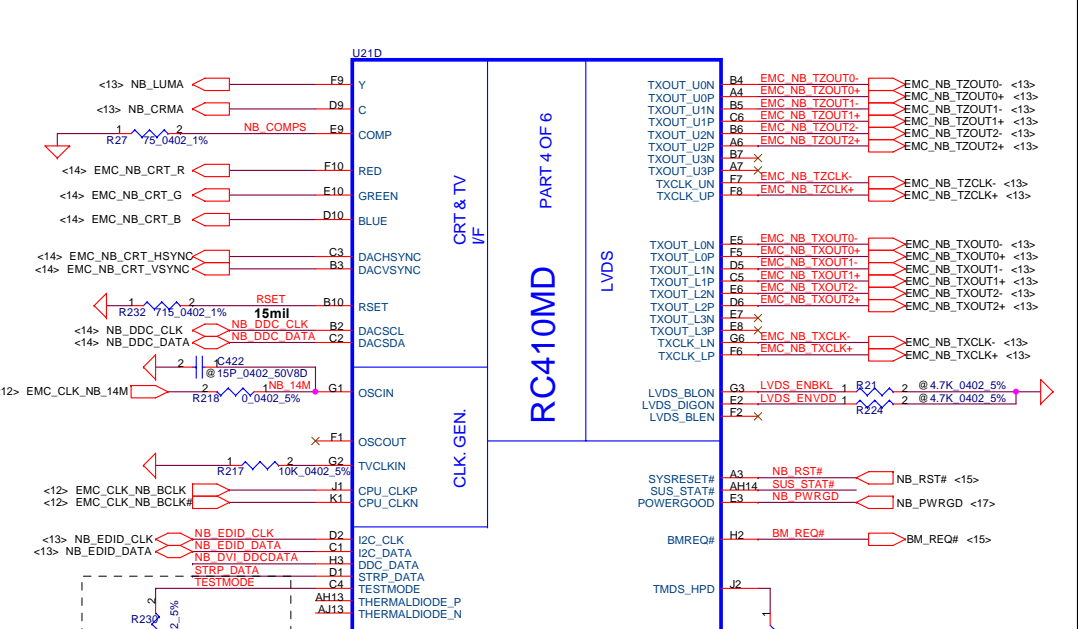
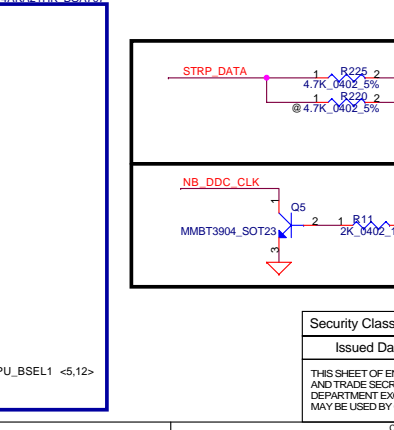
ESR <= 1.5m ohm
Capacitor > 1980uF



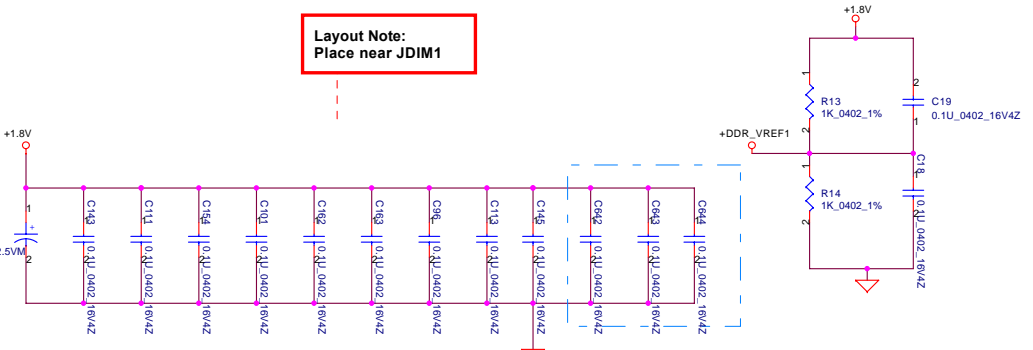
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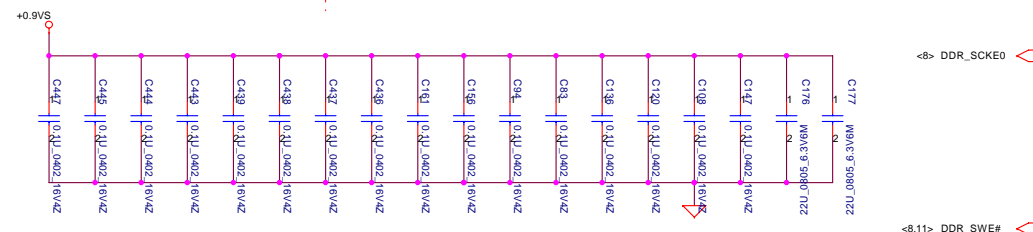
ADDRESS	CLK	MISC	DATA
MEM_A0			AJ16 DDR D00
MEM_A1			AH16 DDR D01
MEM_A2			AJ19 DDR D02
MEM_A3			AH19 DDR D03
MEM_A4			AH15 DDR D04
MEM_A5			AK16 DDR D05
MEM_A6			AH18 DDR D06
MEM_A7			AK19 DDR D07
MEM_A8			AH19 DDR D08
MEM_A9			AE19 DDR D09
MEM_A10			AE19 DDR D10
MEM_A11			AF19 DDR D11
MEM_A12			AE13 DDR D12
MEM_A13			AG19 DDR D13
MEM_A14			AF18 DDR D14
MEM_A15			AE18 DDR D15
MEM_A16			AF20 DDR D16
MEM_A17			AG23 DDR D18
MEM_DQ0			AF24 DDR D019
MEM_DQ1			AG19 DDR D20
MEM_DQ2			AG20 DDR D21
MEM_DQ3			AG22 DDR D22
MEM_DQ4			AF23 DDR D23
MEM_DQ5			AG25 DDR D25
MEM_DQ6			AD25 DDR D24
MEM_DQ7			AD27 DDR D27
MEM_DQ8			AE23 DDR D28
MEM_DQ9			AD24 DDR D29
MEM_DQ10			AE26 DDR D30
MEM_DQ11			AD26 DDR D31
MEM_DQ12			AA25 DDR D32
MEM_DQ13			Y26 DDR D33
MEM_DQ14			W24 DDR D34
MEM_DQ15			LU25 DDR D35
MEM_DQ16			AA26 DDR D36
MEM_DQ17			Y25 DDR D37
MEM_DQ18			V26 DDR D38
MEM_DQ19			AD36 DDR D44
MEM_DQ20			AD29 DDR D45
MEM_DQ21			AA30 DDR D46
MEM_DQ22			Y28 DDR D47
MEM_DQ23			LU27 DDR D48
MEM_DQ24			TZ7 DDR D49
MEM_DQ25			N26 DDR D50
MEM_DQ26			M27 DDR D51
MEM_DQ27			T26 DDR D52
MEM_DQ28			P27 DDR D54
MEM_DQ29			P26 DDR D55
MEM_DQ30			LU29 DDR D56
MEM_DQ31			T29 DDR D57
MEM_DQ32			P29 DDR D58
MEM_DQ33			N29 DDR D59
MEM_DQ34			LU28 DDR D60
MEM_DQ35			T28 DDR D61
MEM_DQ36			P28 DDR D62
MEM_DQ37			MEM_DQ62
MEM_DQ38			MEM_DQ63
MEM_DQ39			
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MEM_DQ56			
MEM_DQ57			
MEM_DQ58			
MEM_DQ59			
MEM_DQ60			
MEM_DQ61			
MEM_DQ62			
MEM_DQ63			
MEM_DM0			AJ17 DDR DM0
MEM_DM1			AG16 DDR DM1
MEM_DM2			AE20 DDR DM2
MEM_DM3			AF25 DDR DM3
MEM_DM4			Y27 DDR DM4
MEM_DM5			AB29 DDR DM5
MEM_DM6			R26 DDR DM6
MEM_DM7			R28 DDR DM7



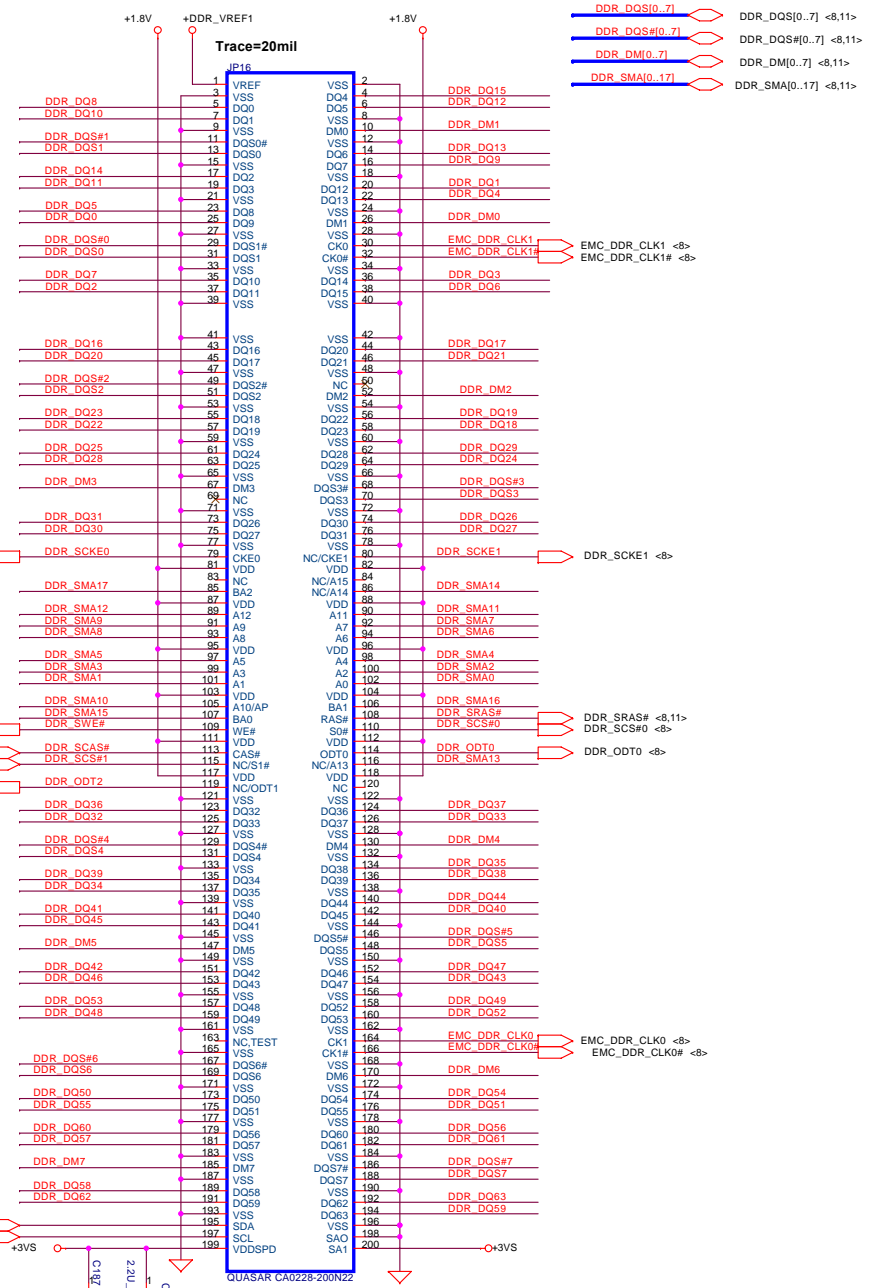
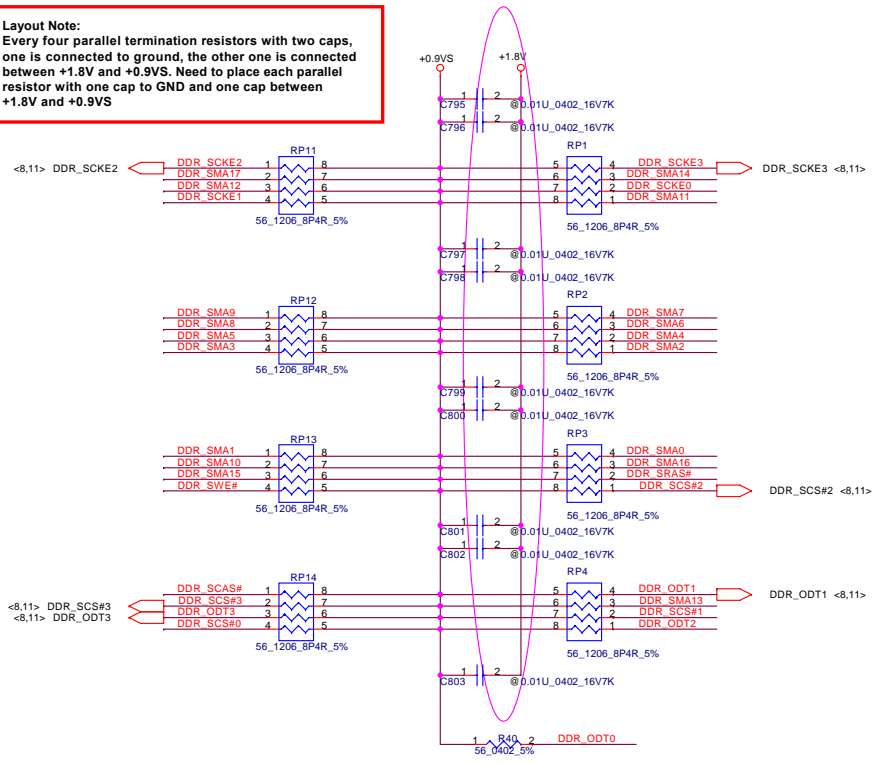
Layout Note:
Place near JDIM1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to V_DDR_MCH_REF



Layout Note:
Every four parallel termination resistors with two caps, one is connected to ground, the other one is connected between +1.8V and +0.9VS. Need to place each parallel resistor with one cap to GND and one cap between +1.8V and +0.9VS



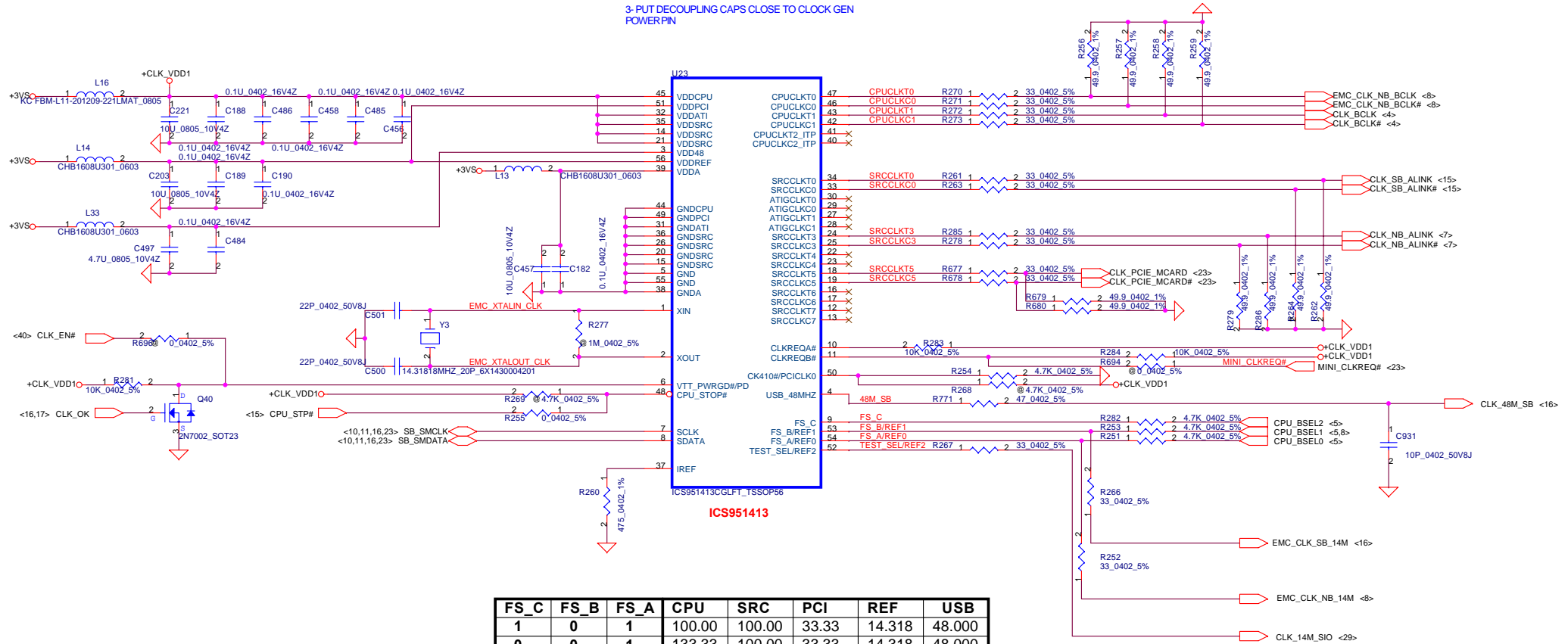
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- DDR_DQS[0..7] <8,11>
- DDR_DQS#0[0..7] <8,11>
- DDR_DM[0..7] <8,11>
- DDR_SMA[0..17] <8,11>

DIMMA Reverse

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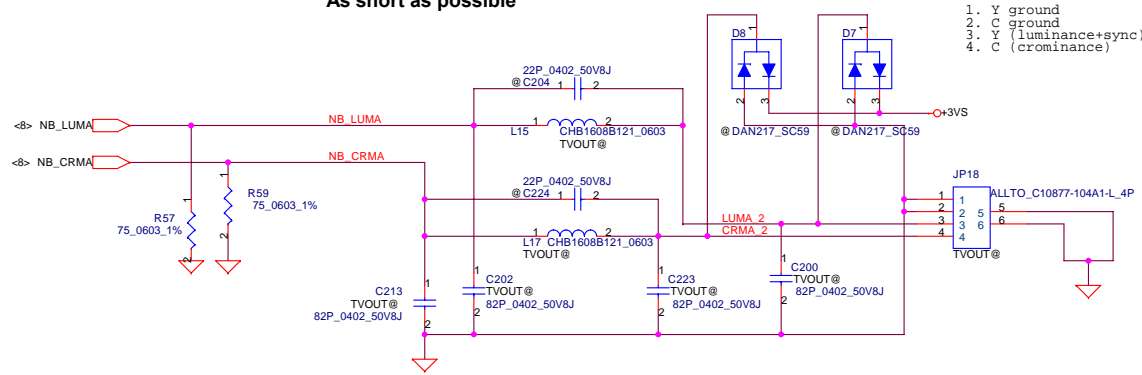
Clock Generator

- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLOCK GEN AS POSSIBLE
- 2- ROUTE ALL CPUCLK#/, NBCLK#/, ITPCLK#/, AND SCR#/ AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWERPIN

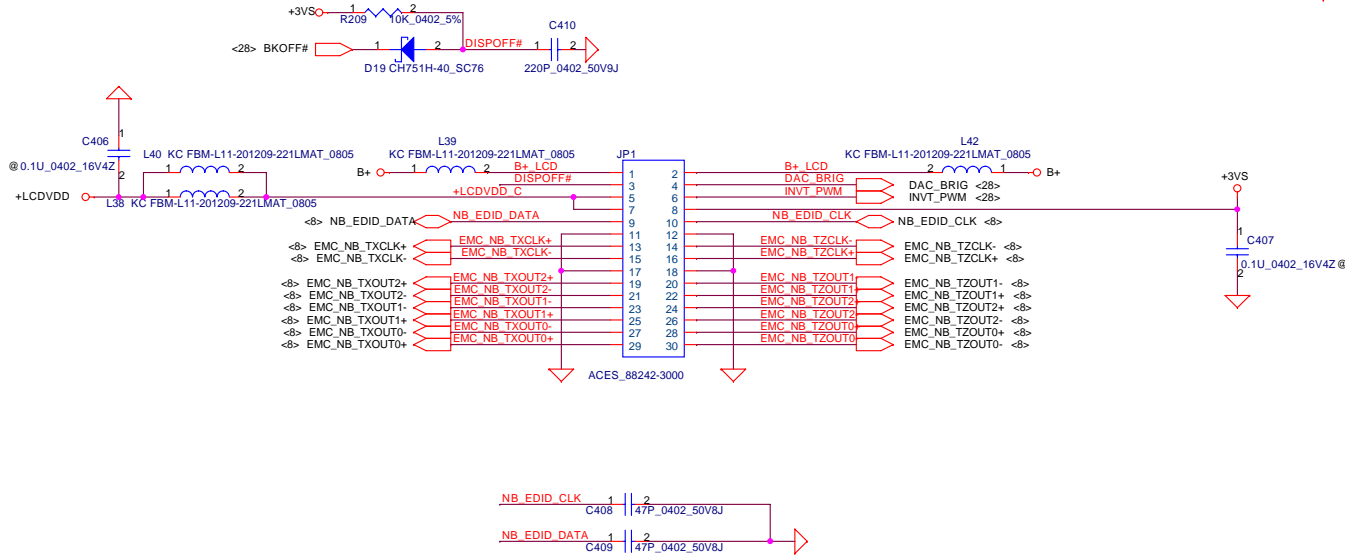


TV-OUT CONNECTOR

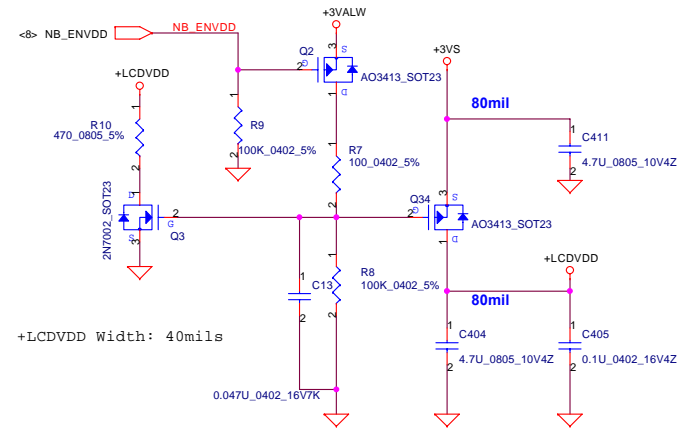
Reduce LUMA_1 and CRMA_1 length
As short as possible



LCD/PANEL BD. Conn.

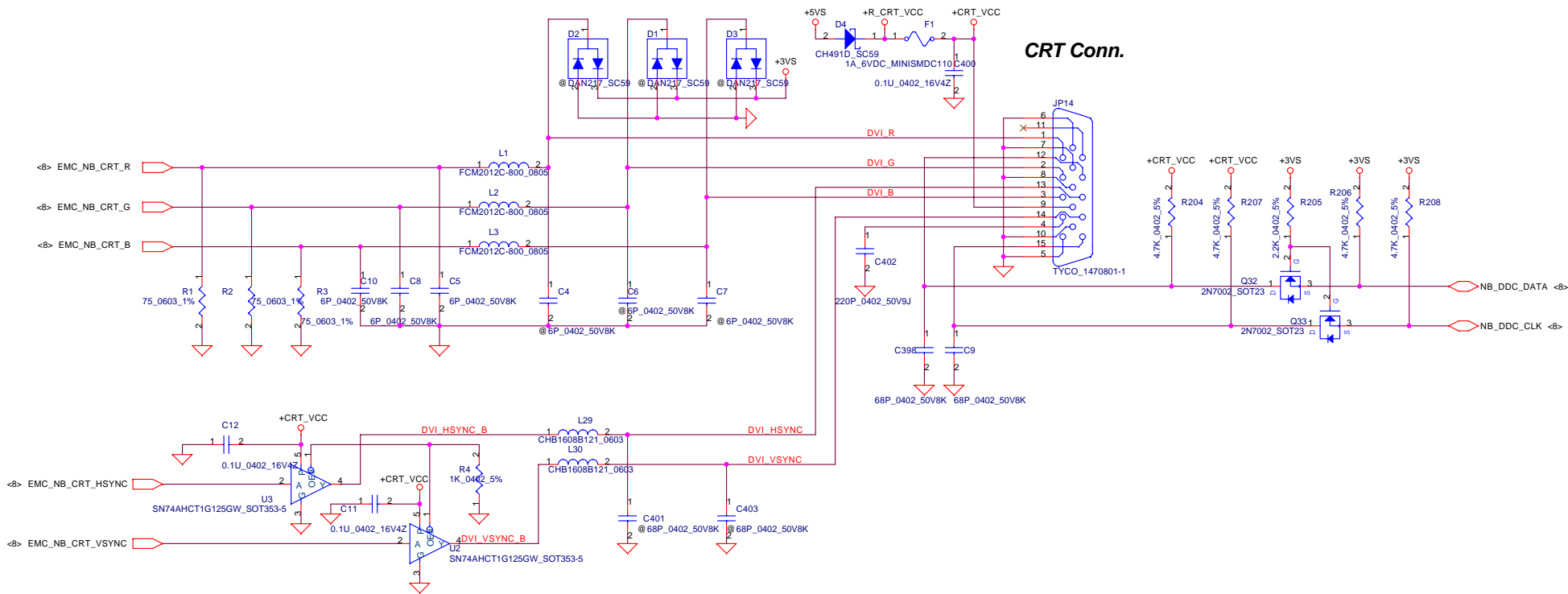


PANEL +LCDVDD CTRL CKT

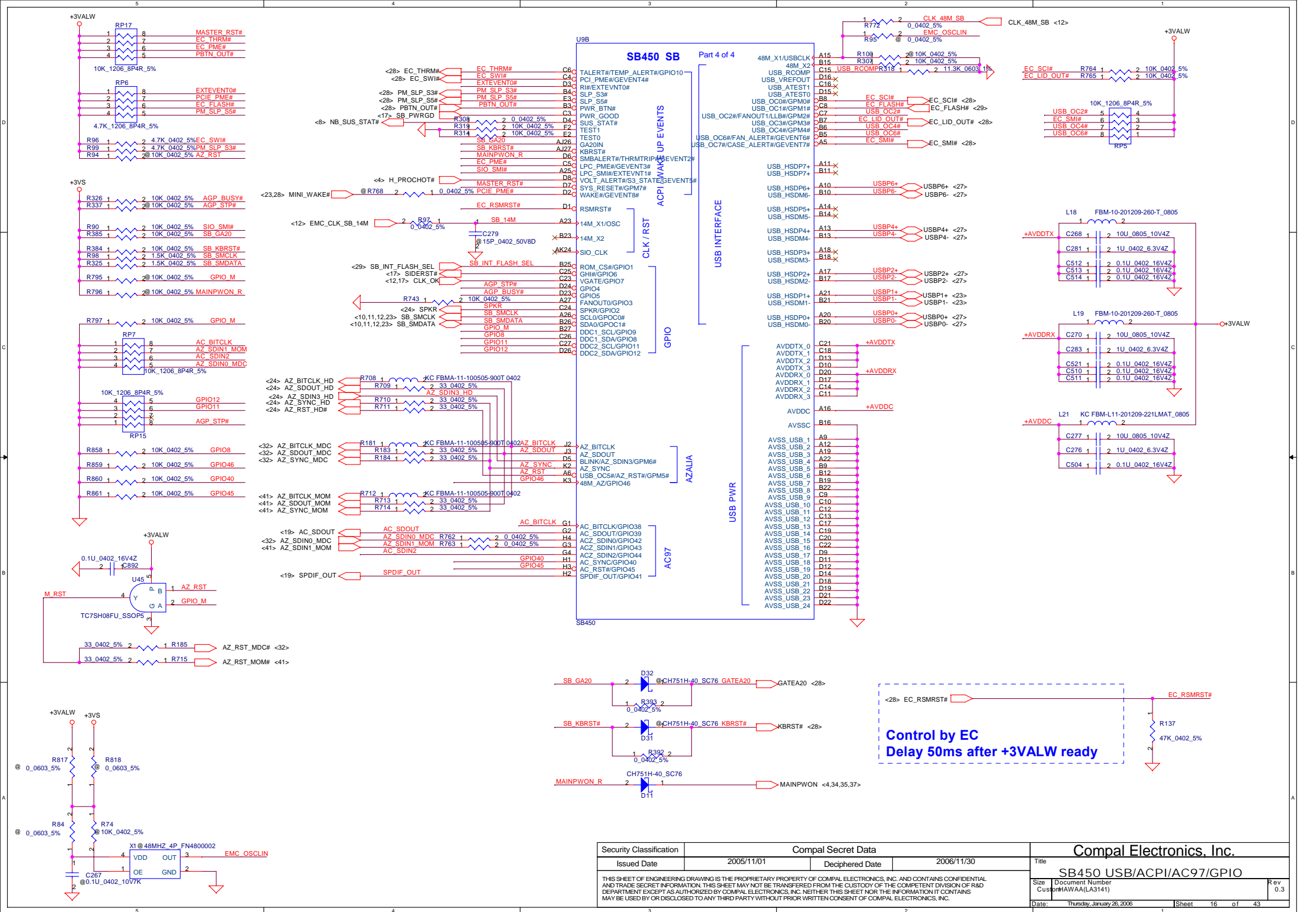


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CRT CONNECTOR

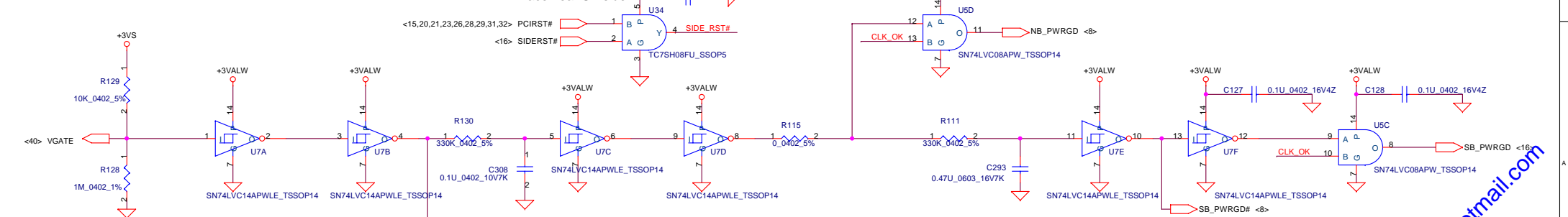
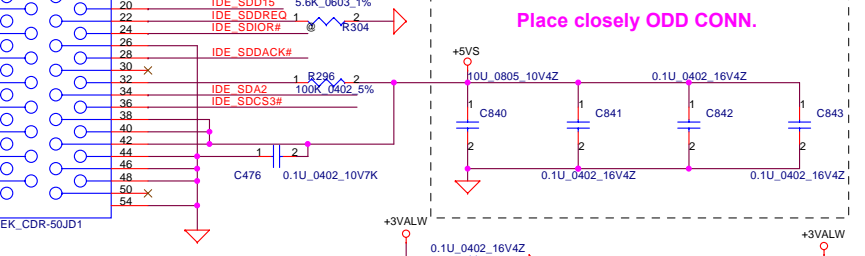
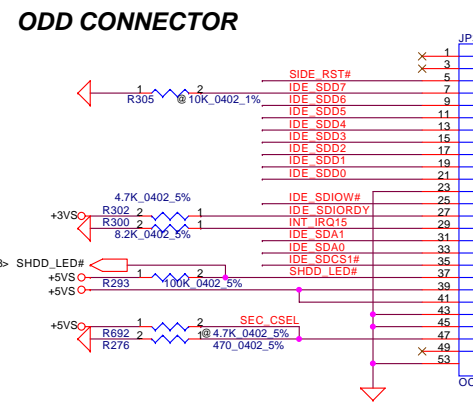
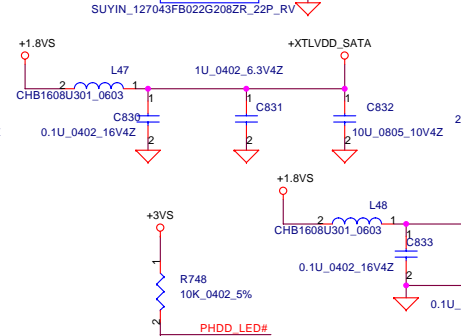
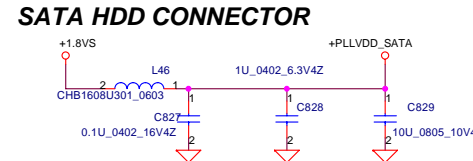
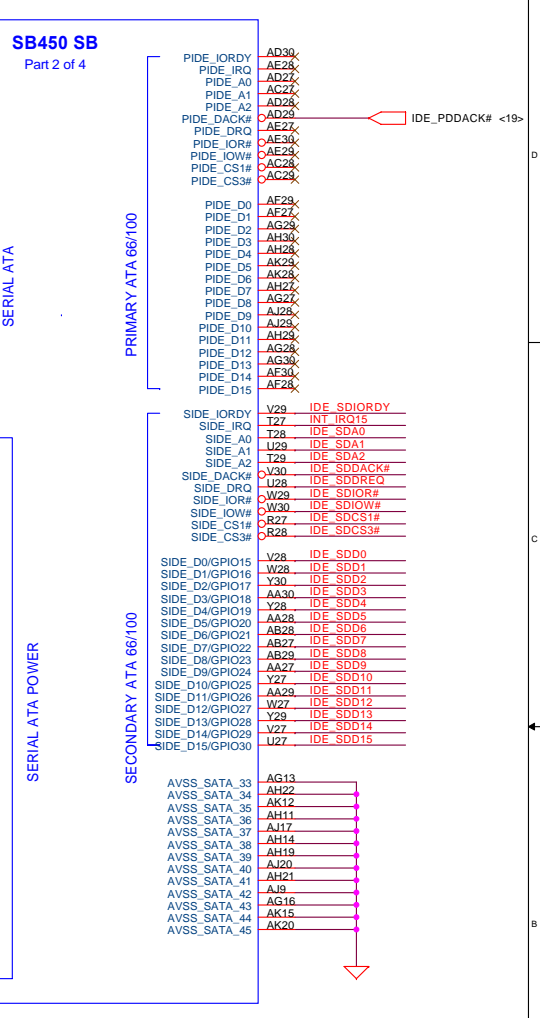
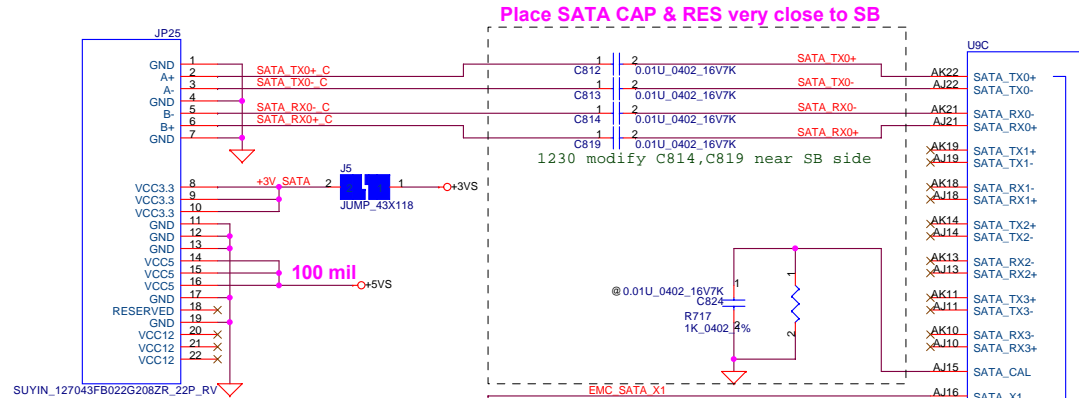
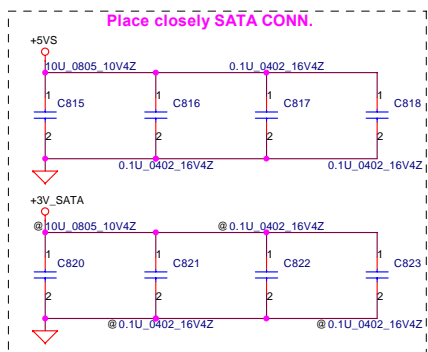


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Date:	Thursday, January 26, 2006	Sheet	14	of	43

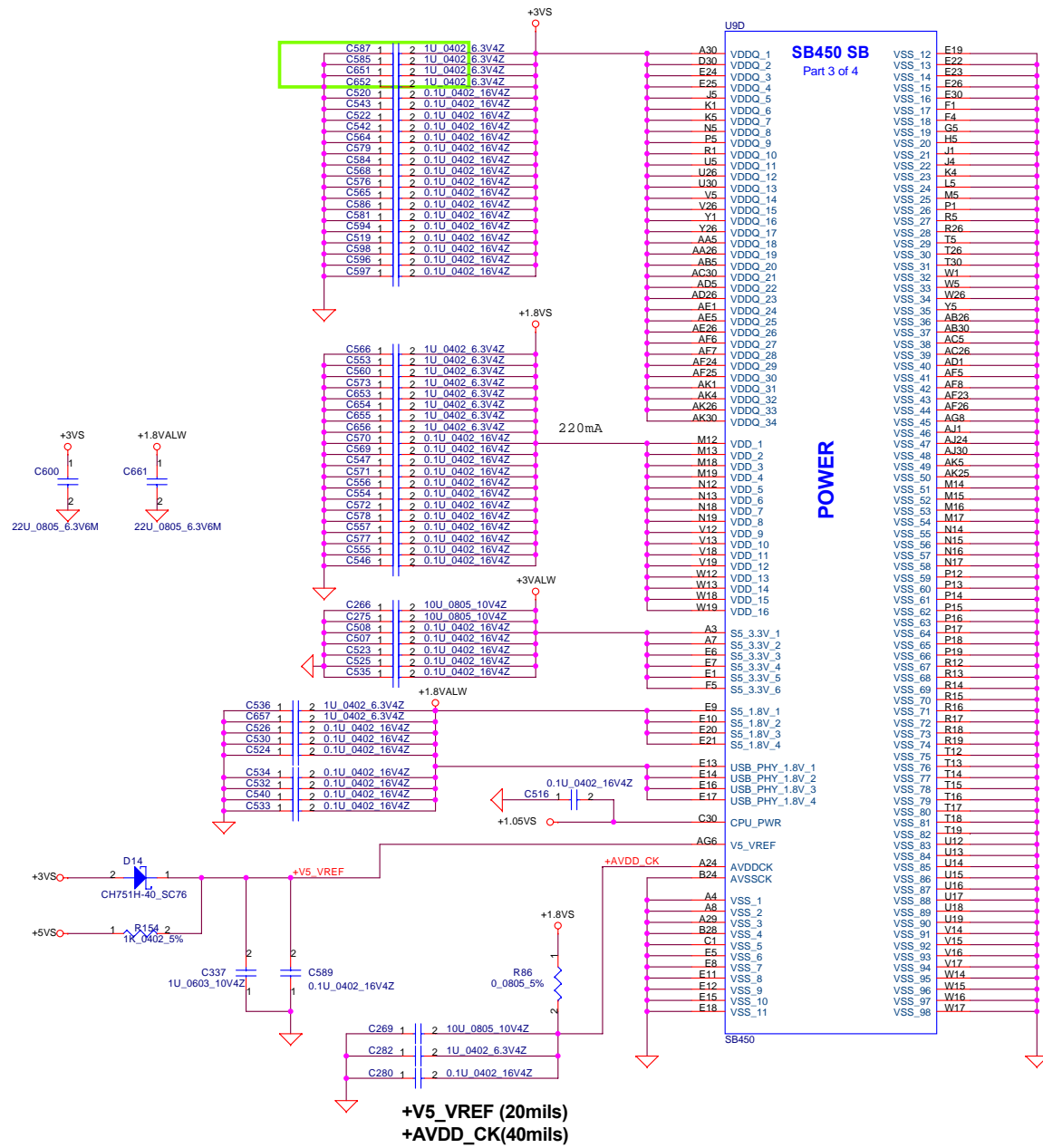


Control by EC
Delay 50ms after +3VALW ready

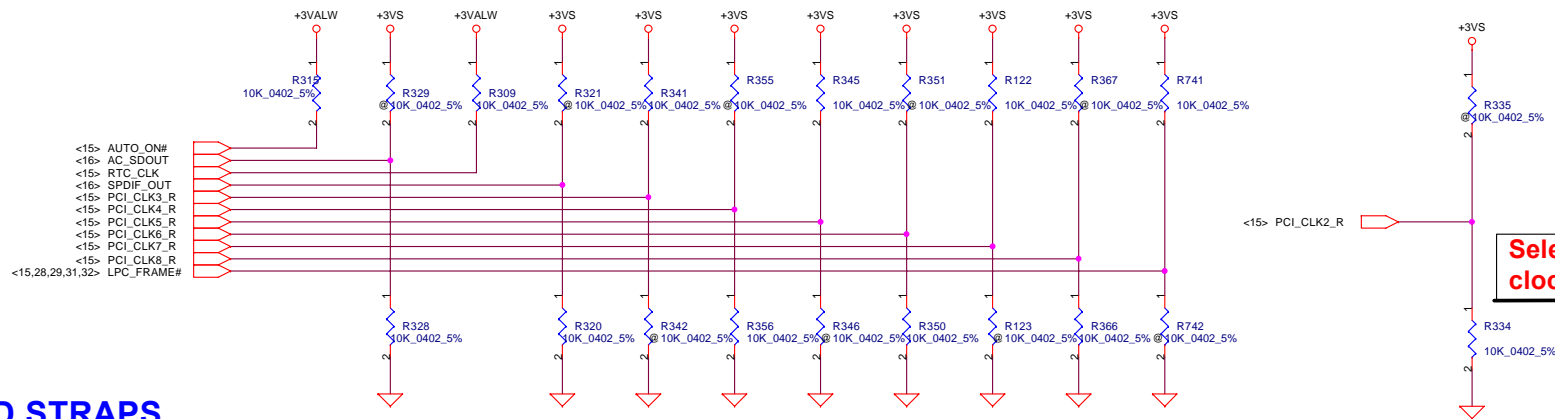
Security Classification	Compal Secret Data		Title	
Issued Date	2005/11/01	Deciphered Date	2006/11/30	SB450 USB/ACPI/AC97/GPIO
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Issued Date	2005/11/01	Deciphered Date	2006/11/30	Title
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Size	Document Number	Rev	Date	Sheet
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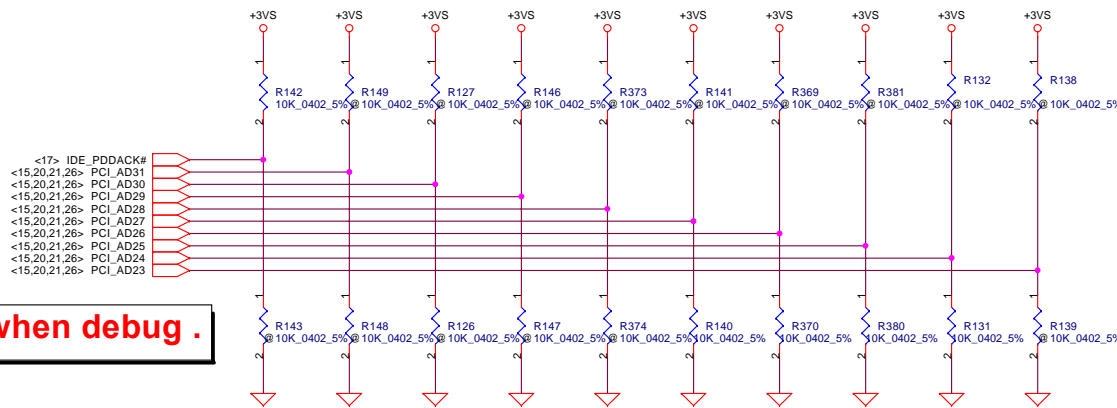
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Issued Date	2005/11/01	Deciphered Date	2006/11/30	Title
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Size	Document Number:	Rev		
Customer	HAWAA(LA3141)	0.3		
Date:	Thursday, January 26, 2006	Sheet	18	of 43



REQUIRED STRAPS

ACPWRON

	AUTO_ON#	AC97_SDOUT	RTC_CLK	SPDIF_OUT	CLK_PCI3	CLK_PCI4	CLK_PCI5	PCI_CLK6	PCI_CLK7	PCI_CLK8	LFRAME#	CLK_PCI2
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	PU for 48MHz XTAL mode	USB PHY PWRDOWN DISABLE DEFAULT	Internal PLL	PCIE AUTO detect DEFAULT	CPU I/F = K8	ROM TYPE H,H = PCI ROM H,L = LPC ROM I L,H = LPC ROM II L,L = FWH ROM		THERMTRIP# ENABLE DEFAULT	Crystal Pad
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	48M OSC mode DEFAULT	USB PHY PWRDOWN ENABLE	External Clock DEFAULT	Forcing PCIE to 2 lanes (debug only)	CPU I/F = P4 DEFAULT			THERMTRIP# DISABLE	Clock input buffer DEFAULT

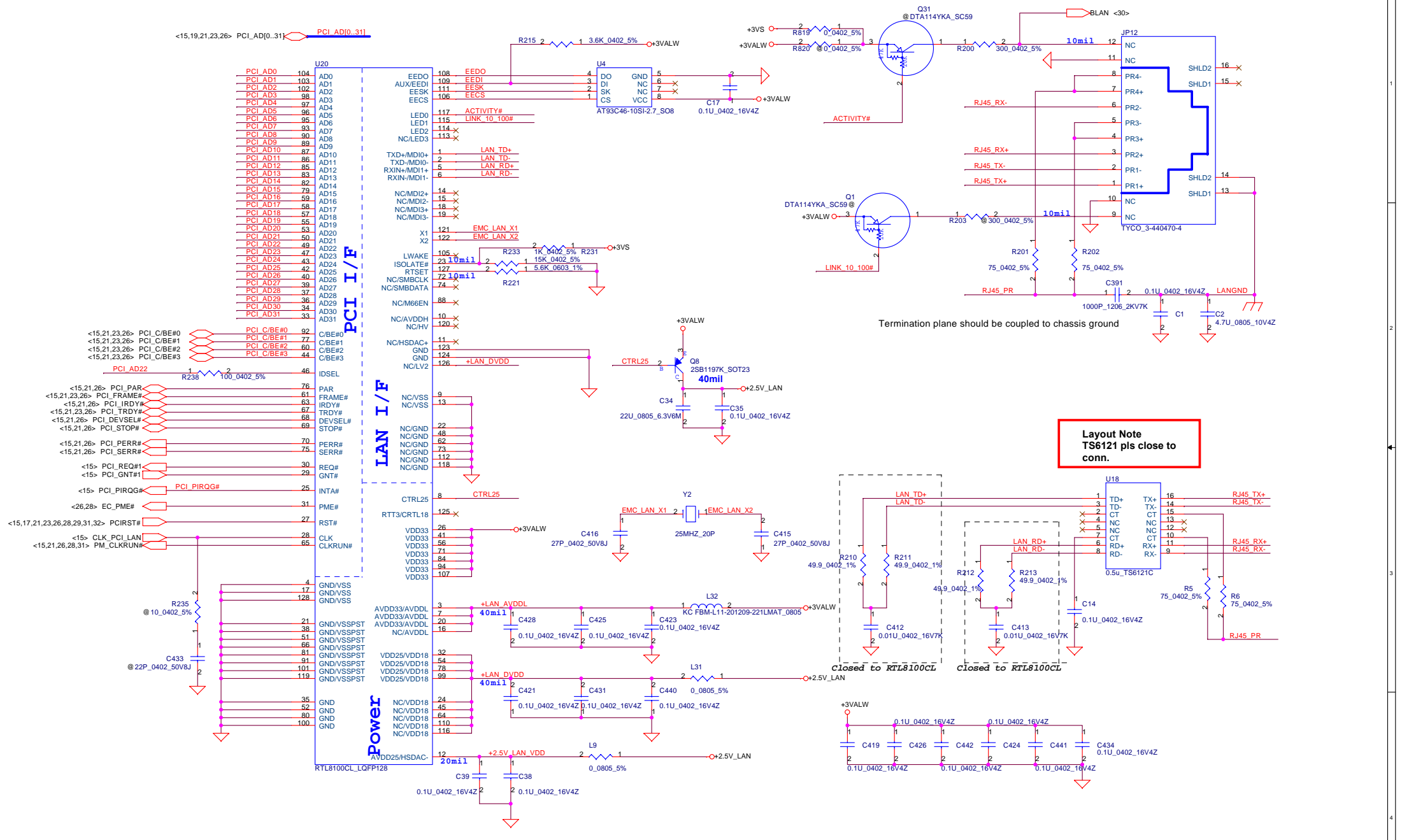


Pop R634 when debug.

DEBUG STRAPS

	IDE_PDDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

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Size	Document Number	Rev		Date	
Cust:brHAWAAA(LA3141)		0.3		Thursday, January 26, 2006	
Sheet			19 of 43		



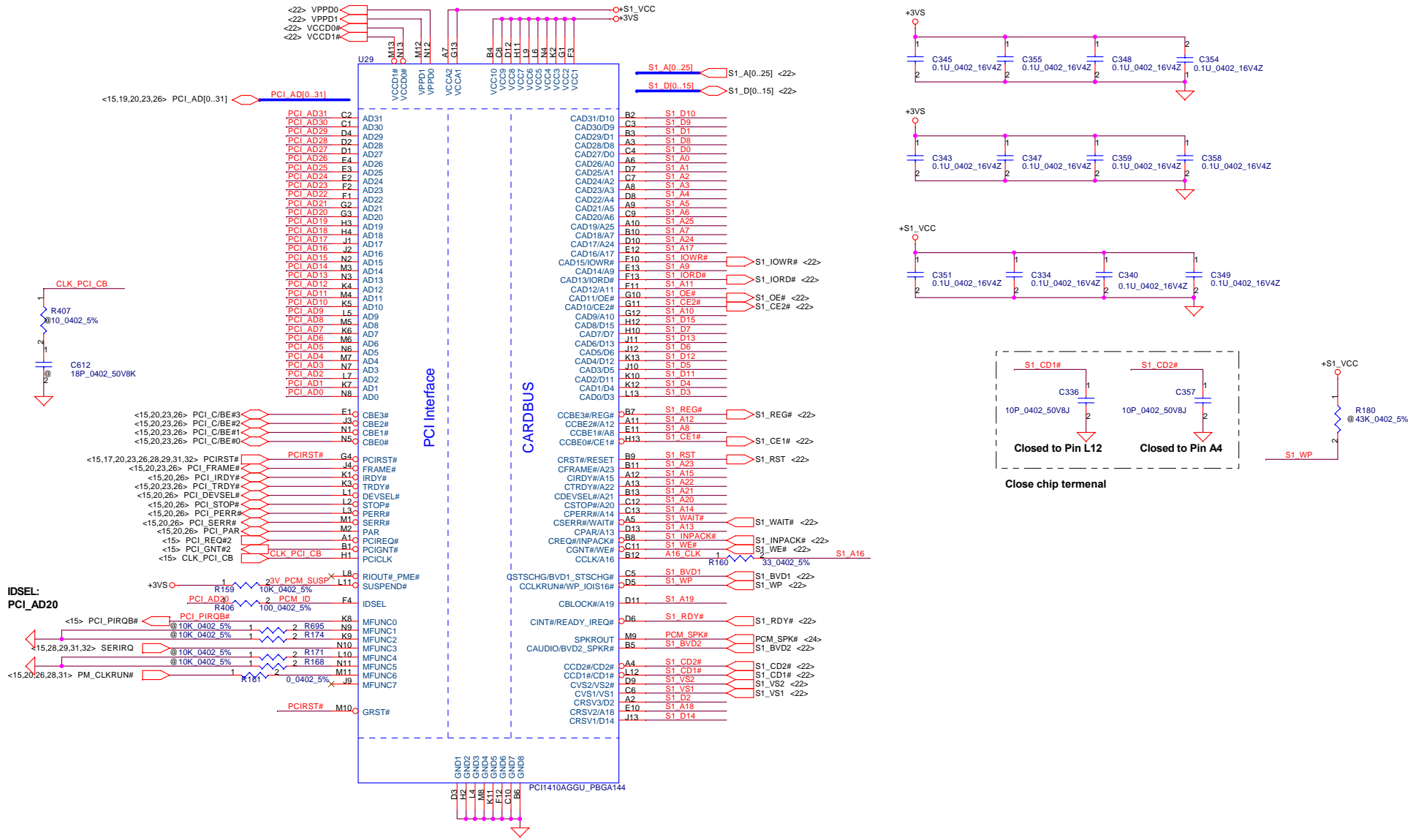
Layout Note
TS6121 pls close to conn.

Termination plane should be coupled to chassis ground

Closed to RTL8100CL

Closed to RTL8100CL

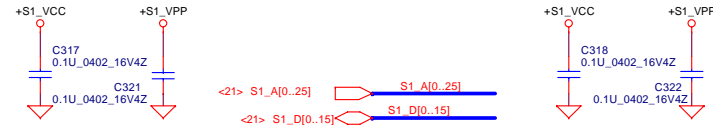
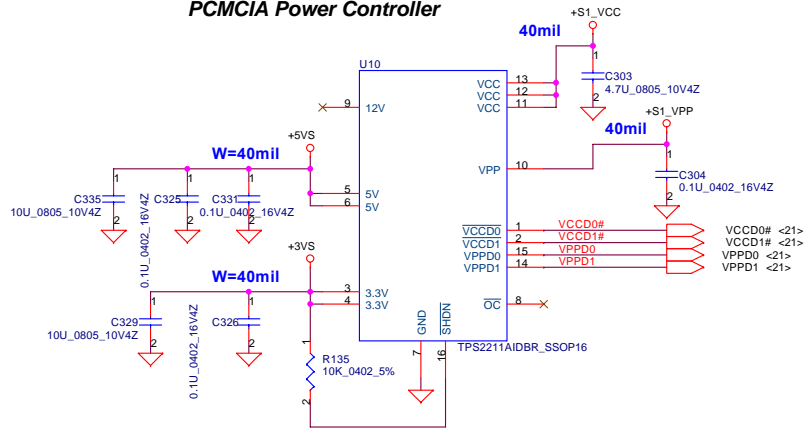
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Date:	Thursday, January 26, 2006	Sheet	20	of 43



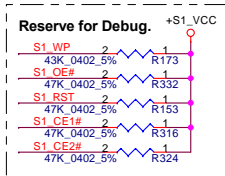
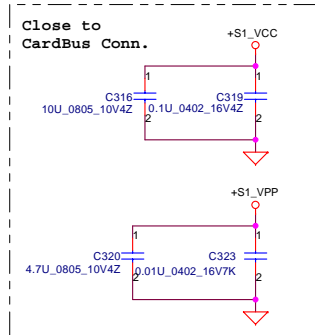
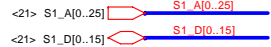
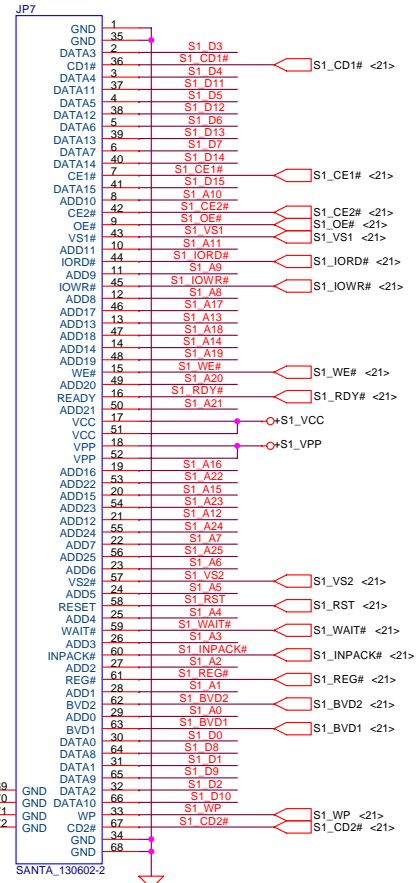
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Size	Document Number	Rev		
Cust	prHAWAA(LA3141)	0.3		
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hexair@outmail.com

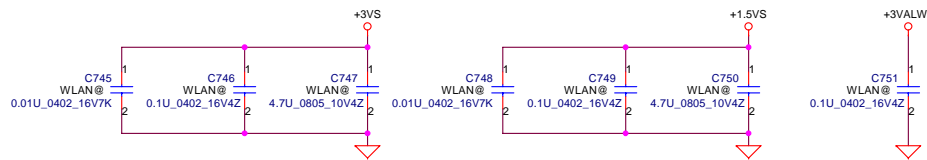
PCMCIA Power Controller



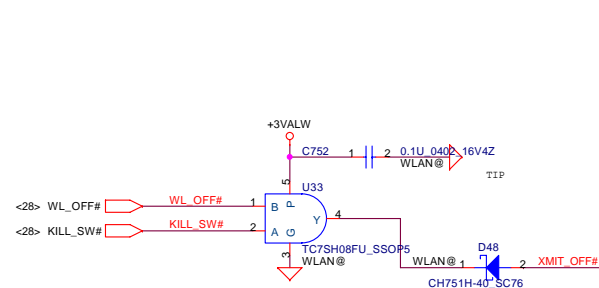
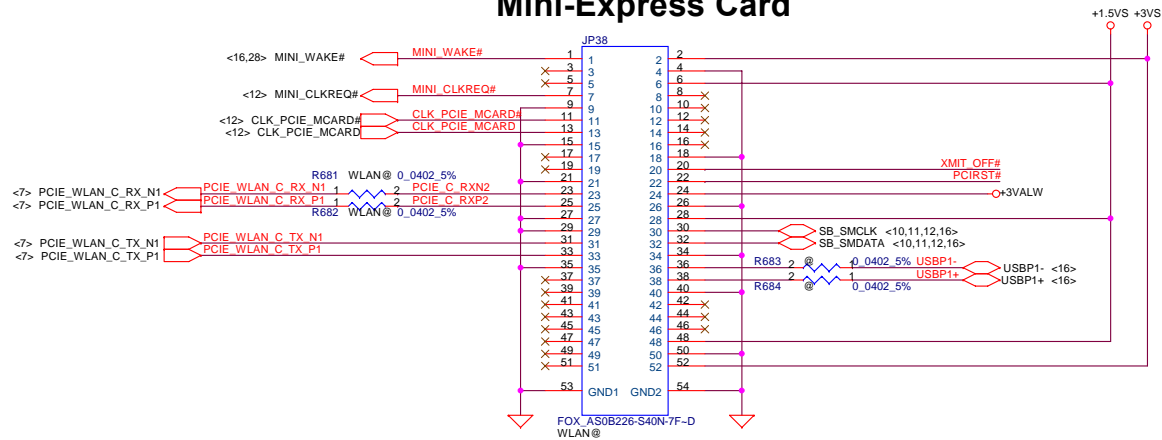
CardBus Socket



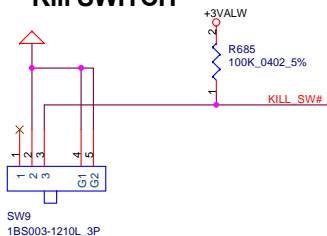
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Issued Date	2005/11/01	Deciphered Date	2006/11/30	Title CARD BUS SOCKET	
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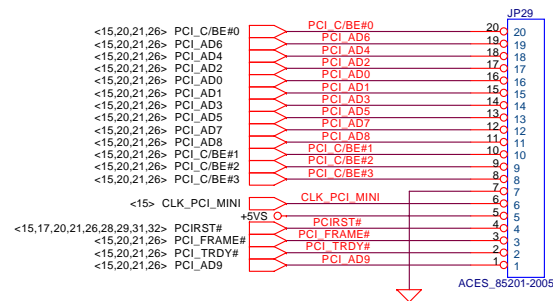
Mini-Express Card



Kill SWITCH



Port 80 Debug Card Connector



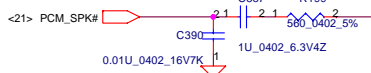
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Size			Document Number	Rev
Cust#			AWAA(LA3141)	0.3
Date:	Thursday, January 26, 2006	Sheet	23	of 43

hexainf@icmail.com

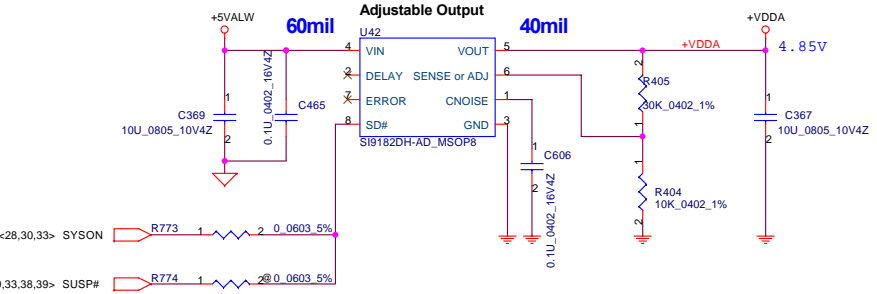
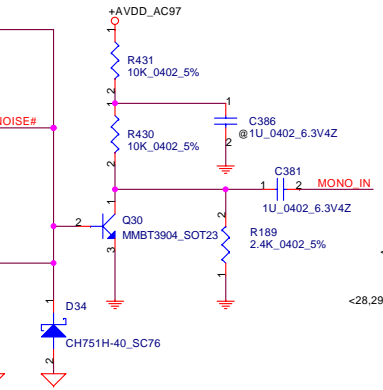
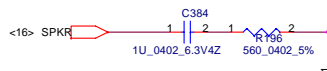
EC Bleep



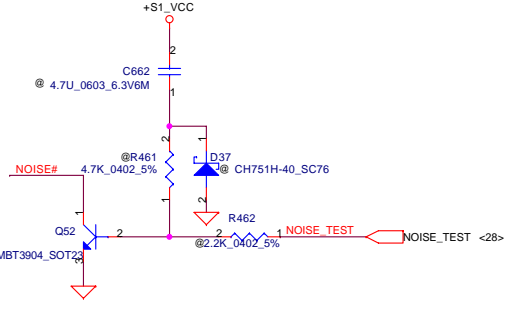
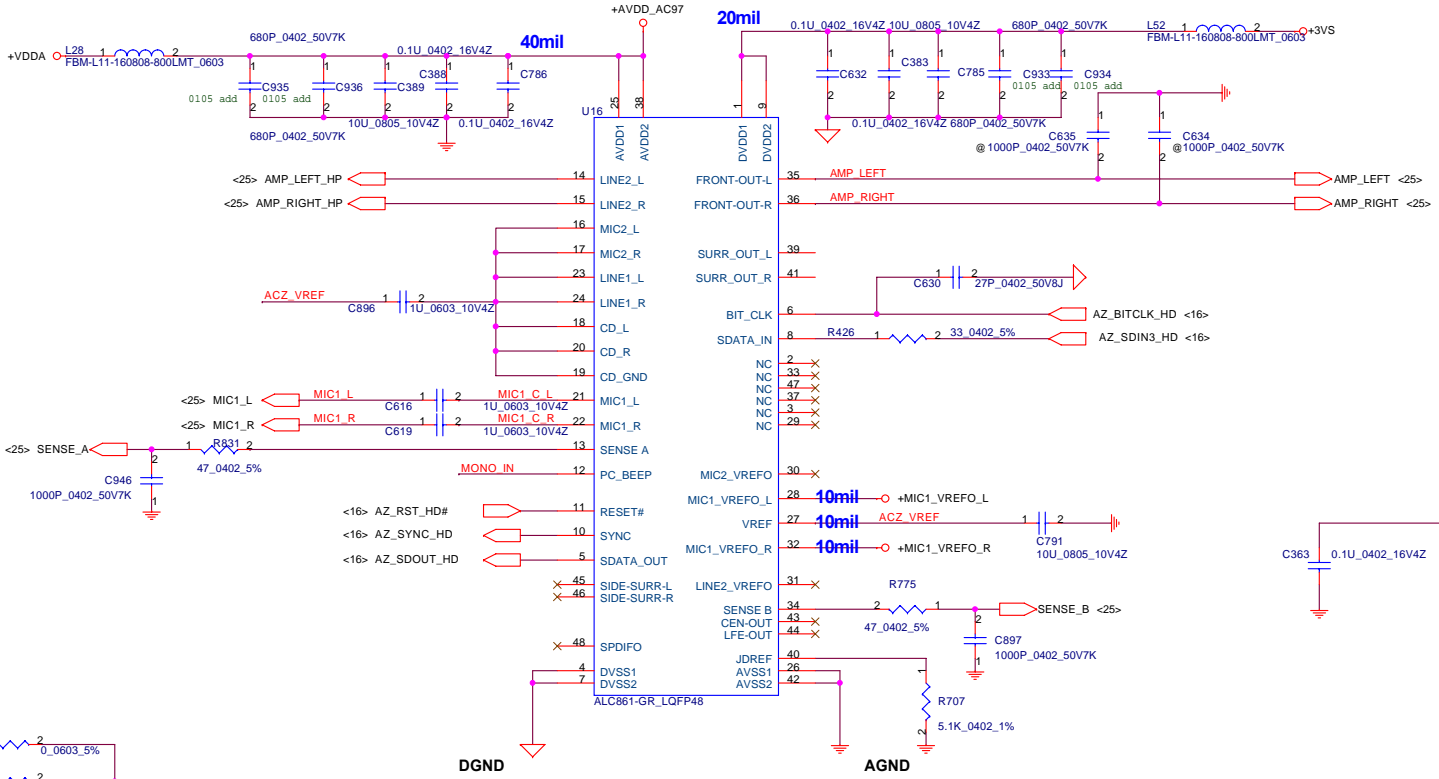
CardBus Bleep



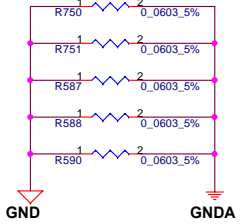
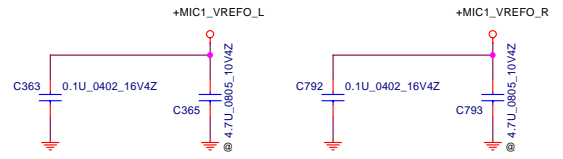
PCI Bleep



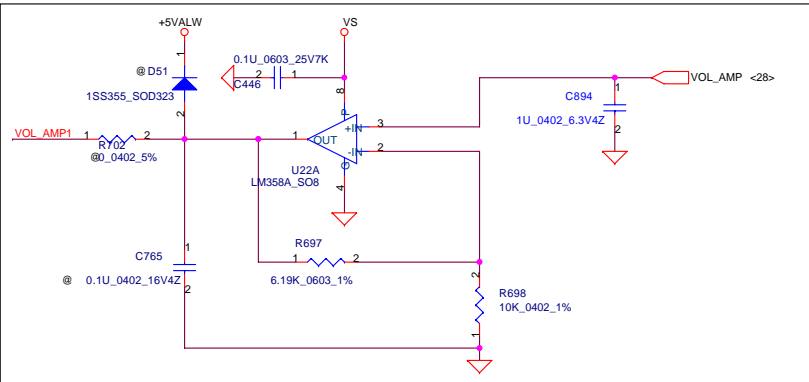
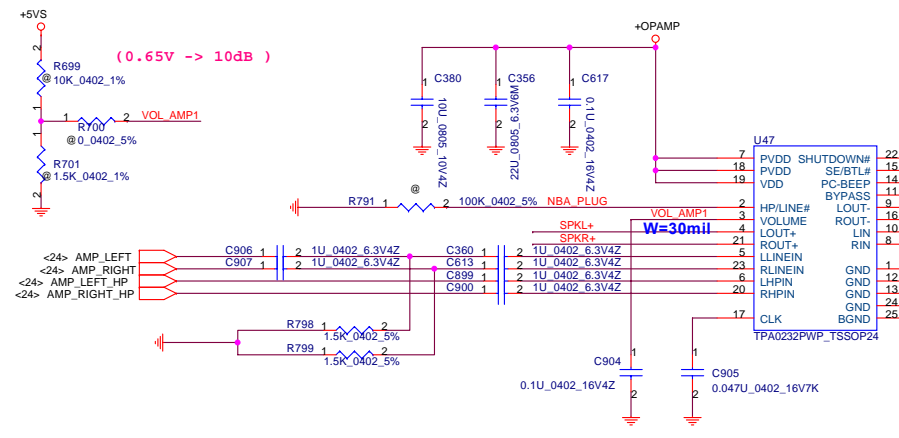
HD Audio Codec



Analog Reference V

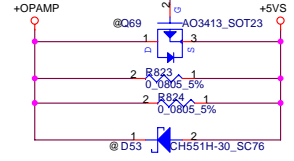
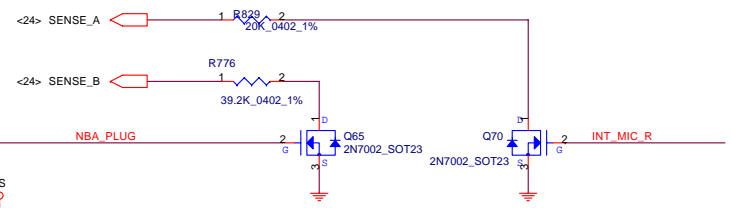
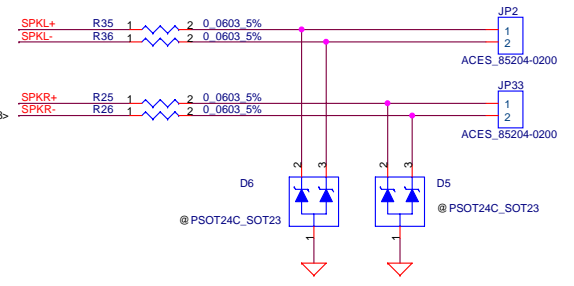


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Size	Document Number	HAWAA(LA3141)		Rev
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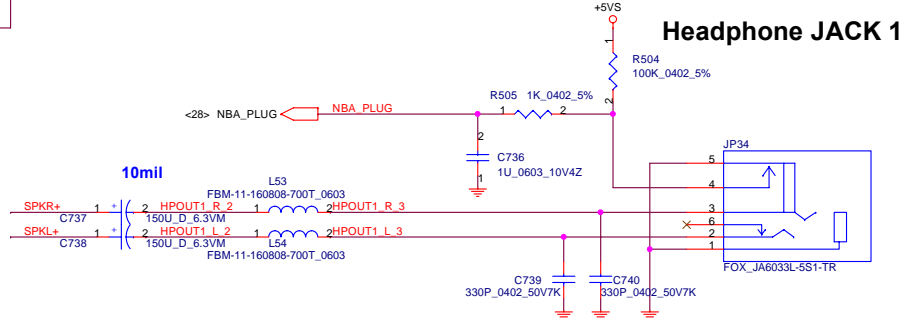


Gain Settings		
	dB	VOL_AMP
SPK	10	0.4V~2.5V
HP	-6	0.75V~2.5V

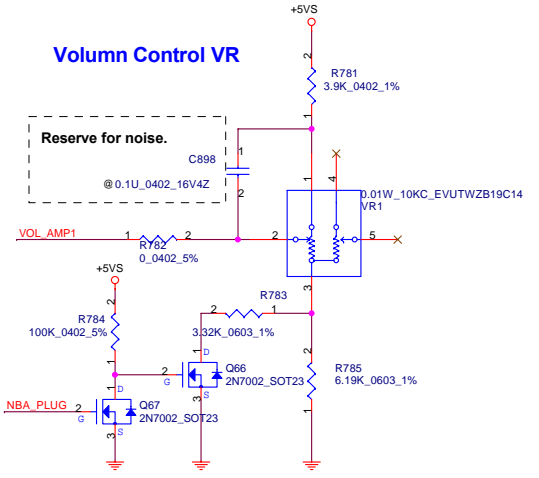
Speaker Conn.



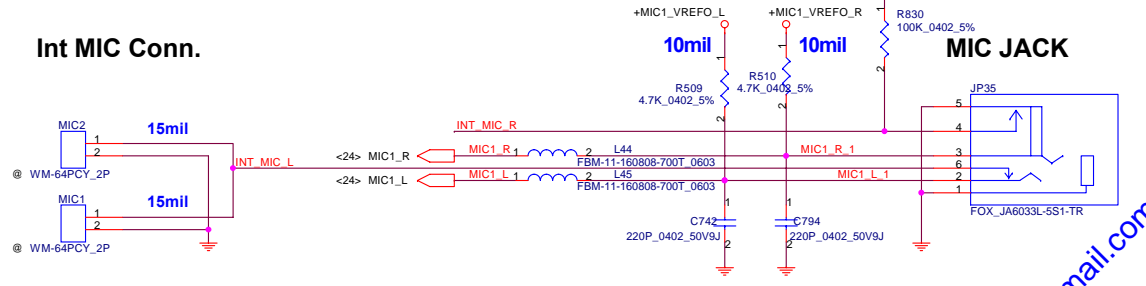
Headphone JACK 1



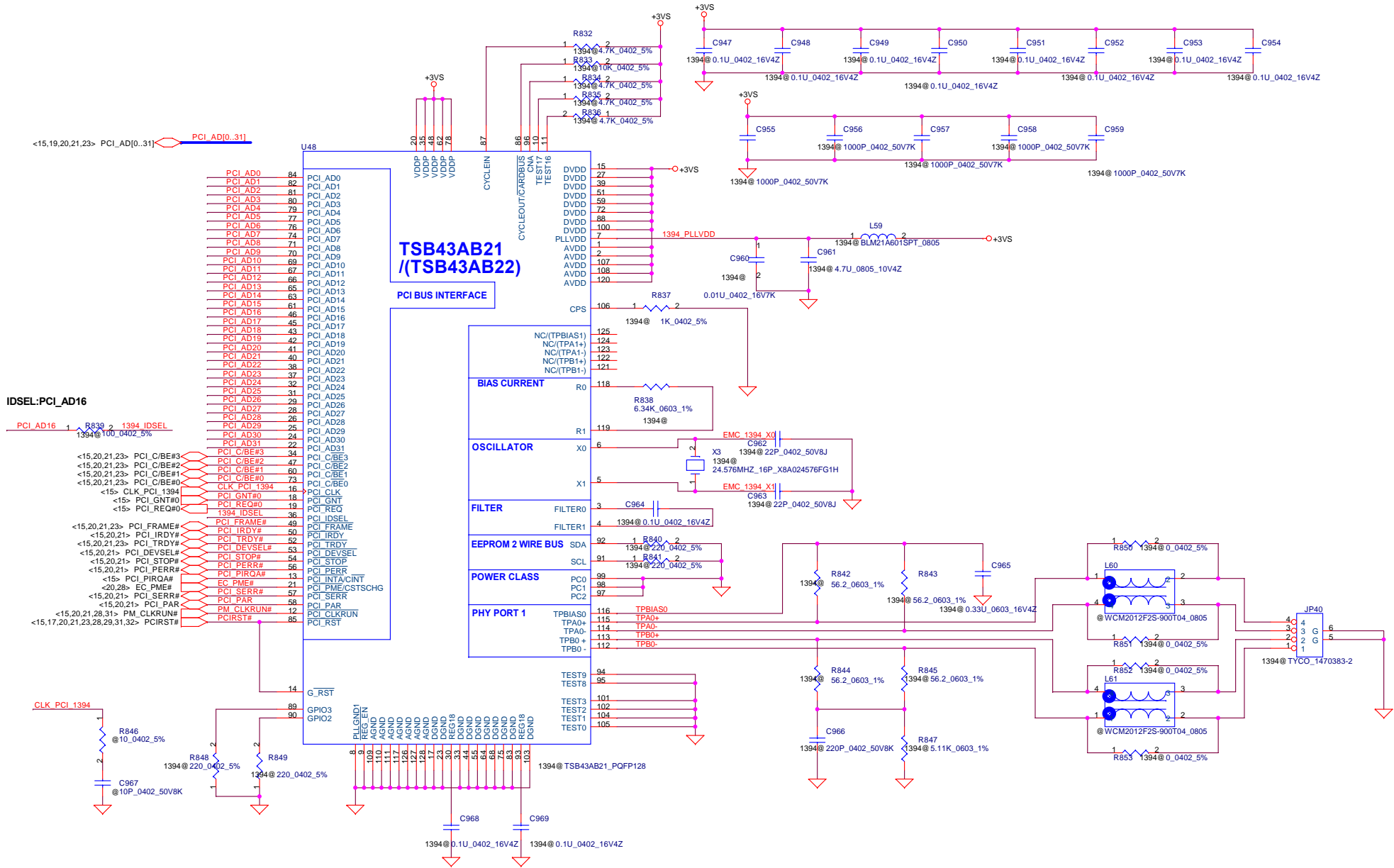
Volume Control VR



Int MIC Conn.



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Size	Document Number	Date	Thursday, January 26, 2006	Rev
	Cust:prhAWAA(LA3141)	Sheet	25 of 43	D.3



<15,19,20,21,23> PCI_AD[0..31] PCI_AD[0..31]

ISSEL:PCI_AD16
 PCI_AD16 1 R839 2 1394 ISSEL
 1394@100_0402_5%

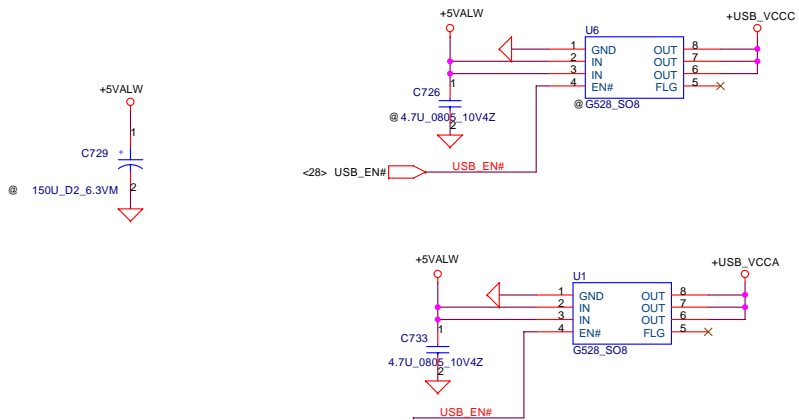
CLK_PCI_1394
 R846 @10_0402_5%
 C967 @10P_0402_50V8K

TSB43AB21 (TSB43AB22)

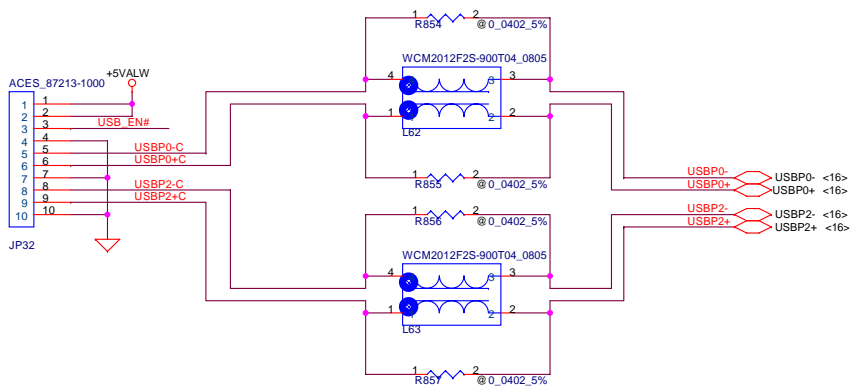
PCI BUS INTERFACE

- NC/(TPBIAS1)
- NC/(TPA1+)
- NC/(TPA1-)
- NC/(TPB1+)
- NC/(TPB1-)
- BIAS CURRENT
- OSCILLATOR
- FILTER
- EEPROM 2 WIRE BUS
- POWER CLASS
- PHY PORT 1

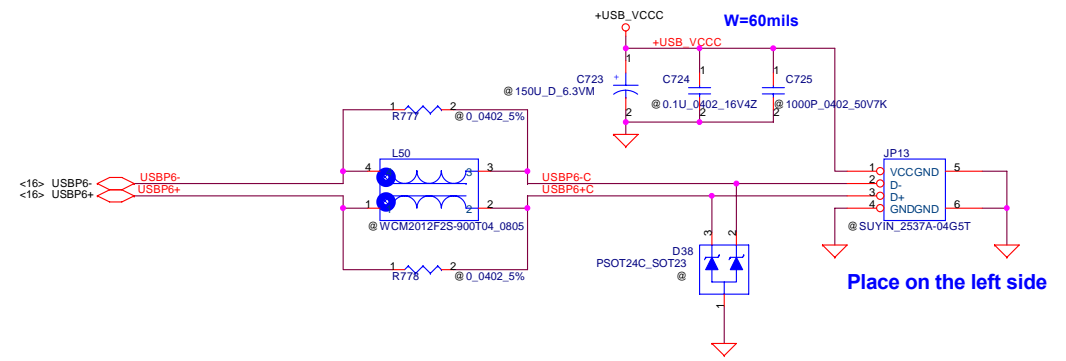
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Size	Document Number	Rev		
Cust	prHA200/BL10E (LA2861)	0.3		
Date:	Thursday, January 26, 2006	Sheet	26	of 43



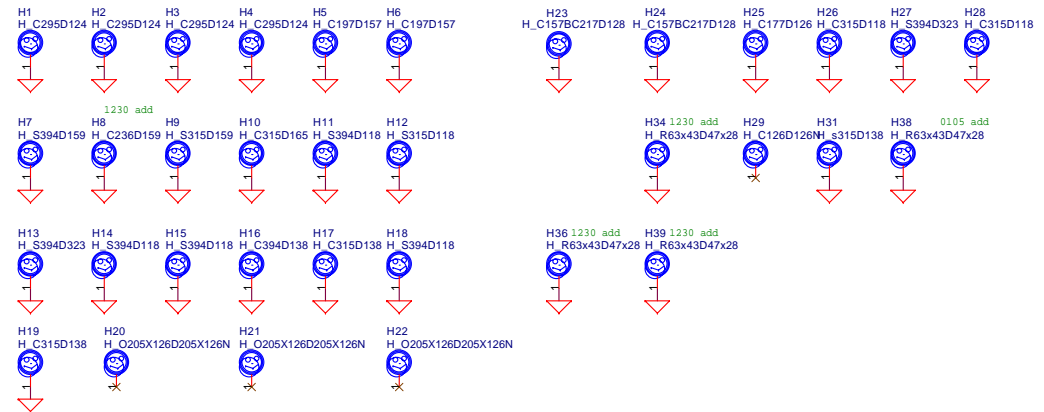
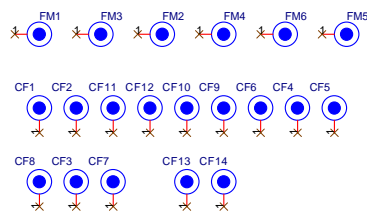
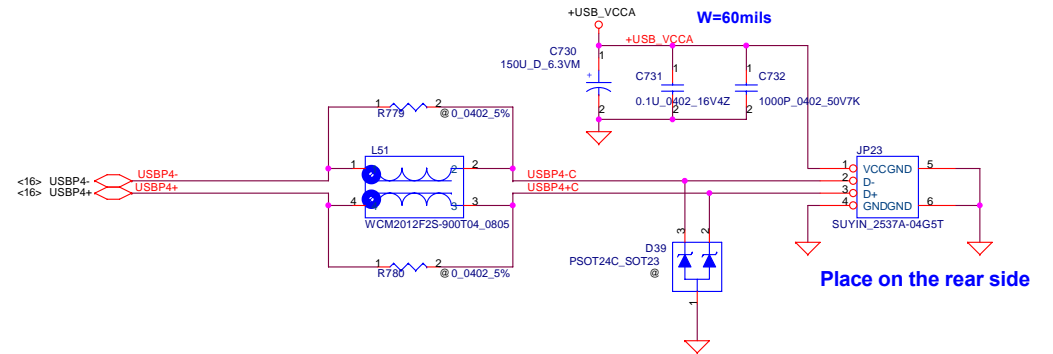
2 port in right side



USB CONN. 1

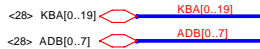
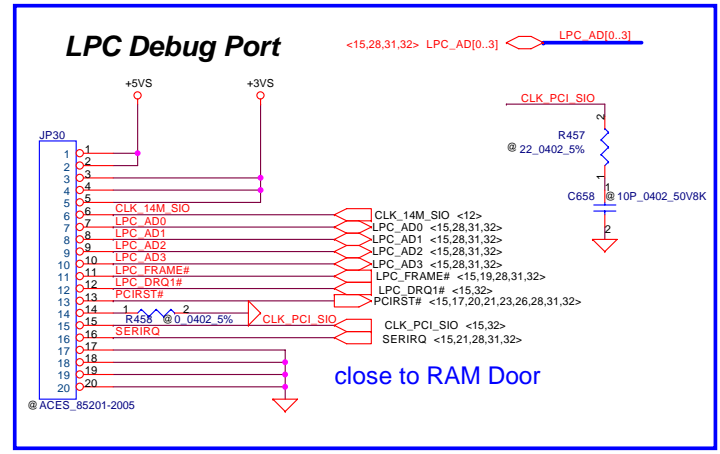
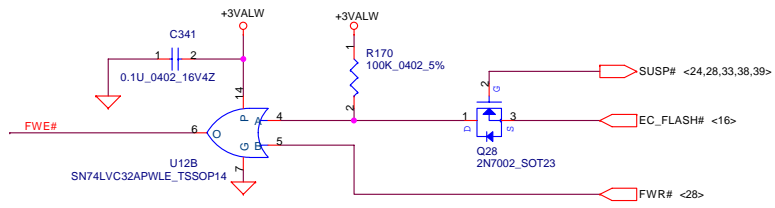
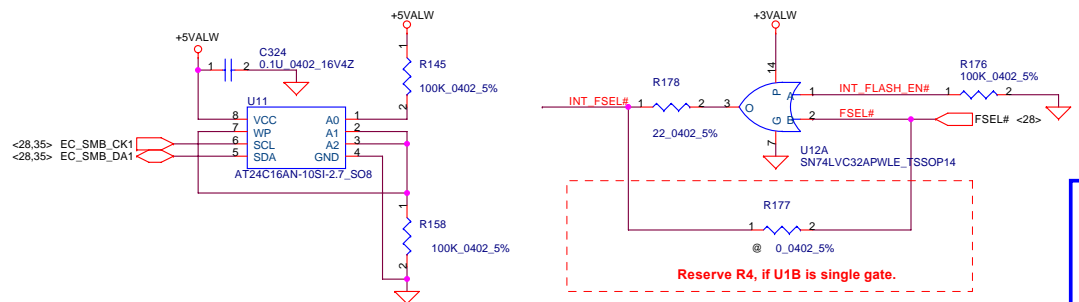


USB CONN.2

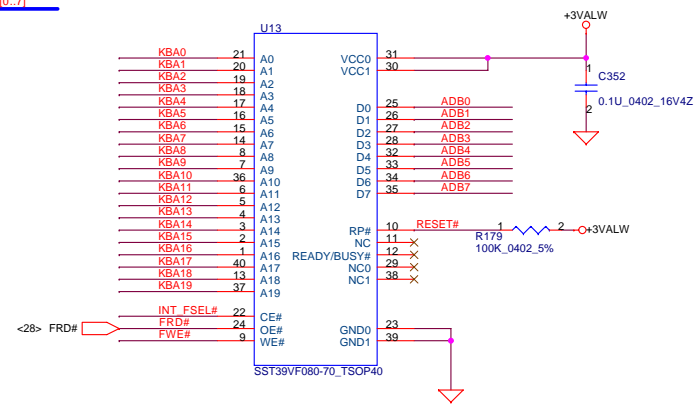


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Size			Document Number	Rev
Date			Customer#	0.2
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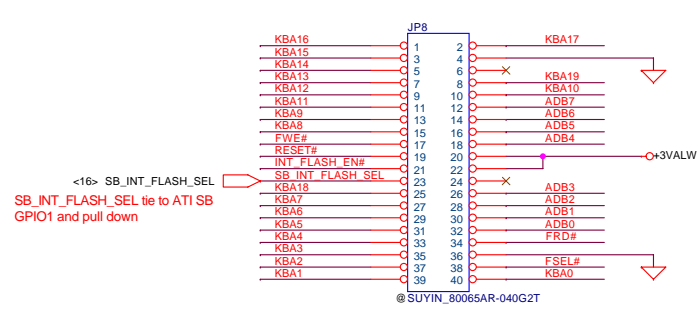
hexrain@hotmail.com



1MB Flash ROM



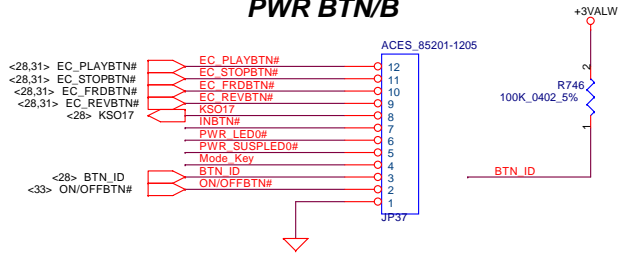
1MB ROM Socket



Security Classification	Compal Secret Data		Title	
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				Document Number
				Customer Part Number
				Revision
				0.3
				Date
				Thursday, January 26, 2006
				Sheet
				29 of 43

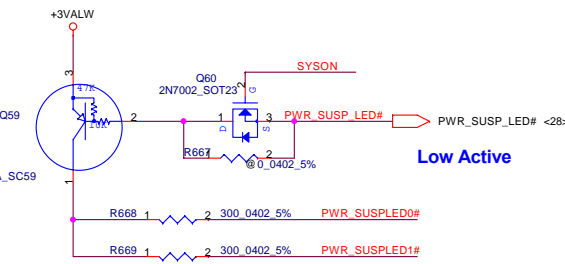
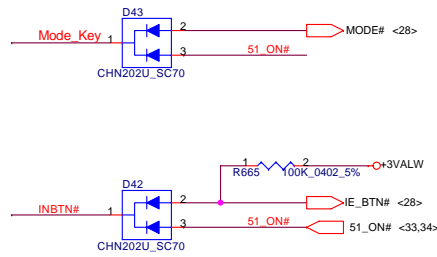
hexainf@gmail.com

PWR BTN/B

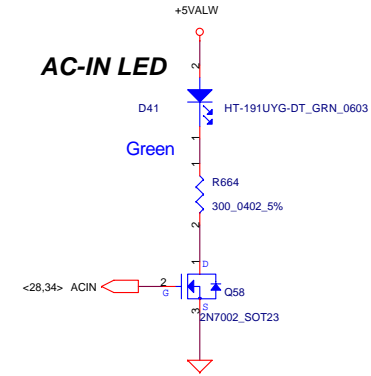


EC_PLAYBTN#	C874	100P_0402_25V8K
EC_STOPBTN#	C875	100P_0402_25V8K
EC_FRDBTN#	C876	100P_0402_25V8K
EC_REVBTN#	C877	100P_0402_25V8K
KSO17	C878	100P_0402_25V8K
INBTN#	C879	100P_0402_25V8K
PWR_LED0#	C880	100P_0402_25V8K
PWR_SUSPLED0#	C881	100P_0402_25V8K
Mode_Key	C882	100P_0402_25V8K
BTN_ID	C883	120P_0402_25V8K
ON/OFFBTN#	C884	120P_0402_25V8K

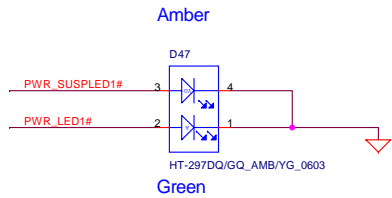
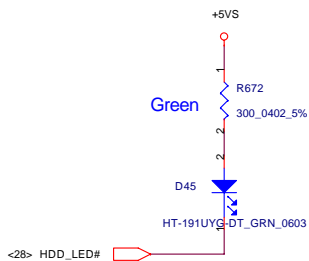
Vivace Button



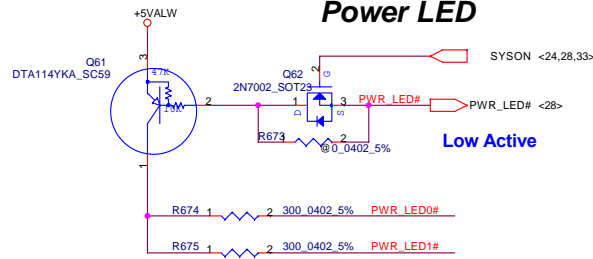
AC-IN LED



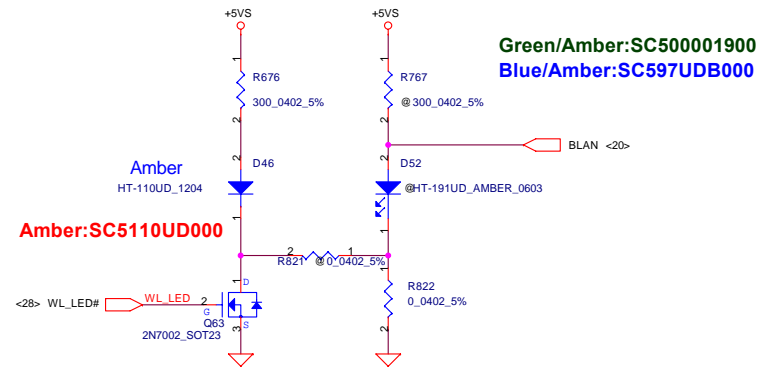
HDD LED



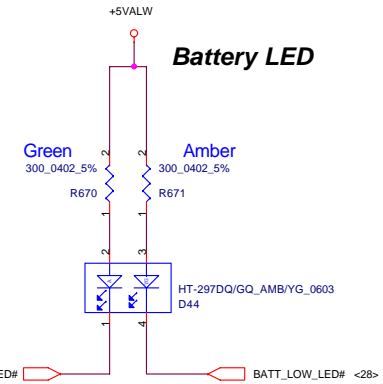
Power LED



Wireless Lan LED

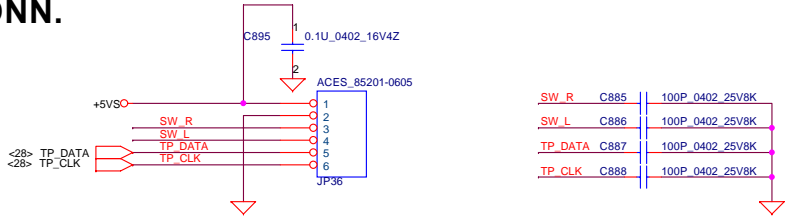


Battery LED



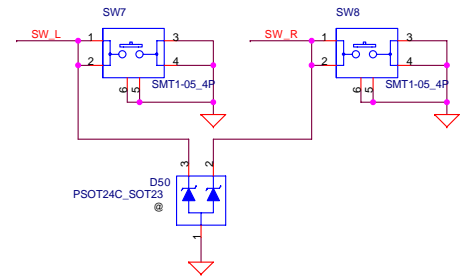
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Size	Document Number	R ev		
Cust:brHAWAA(LA3141)		0.2		
Date:	Thursday, January 26, 2006	Sheet	30 of 43	

TP CONN.



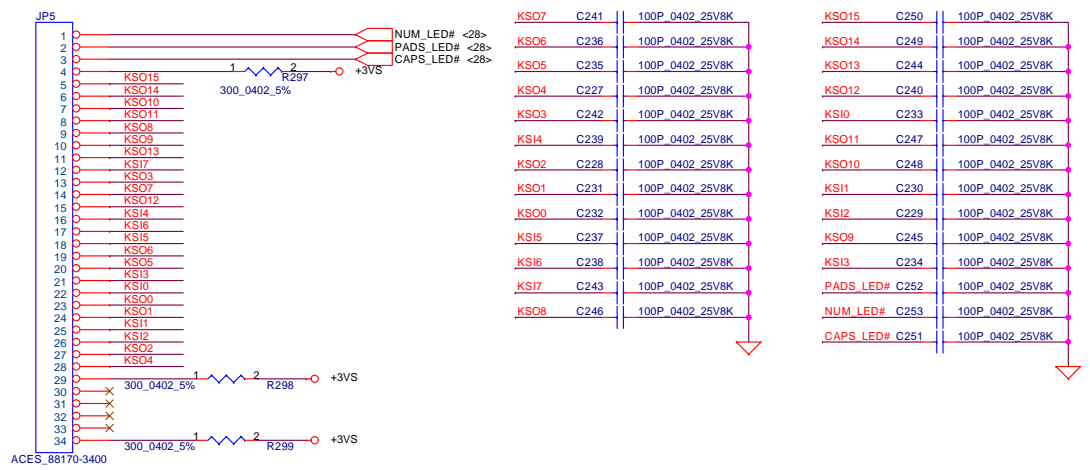
SW_R	C885	100P_0402_25V8K
SW_L	C886	100P_0402_25V8K
TP_DATA	C887	100P_0402_25V8K
TP_CLK	C888	100P_0402_25V8K

TP Button



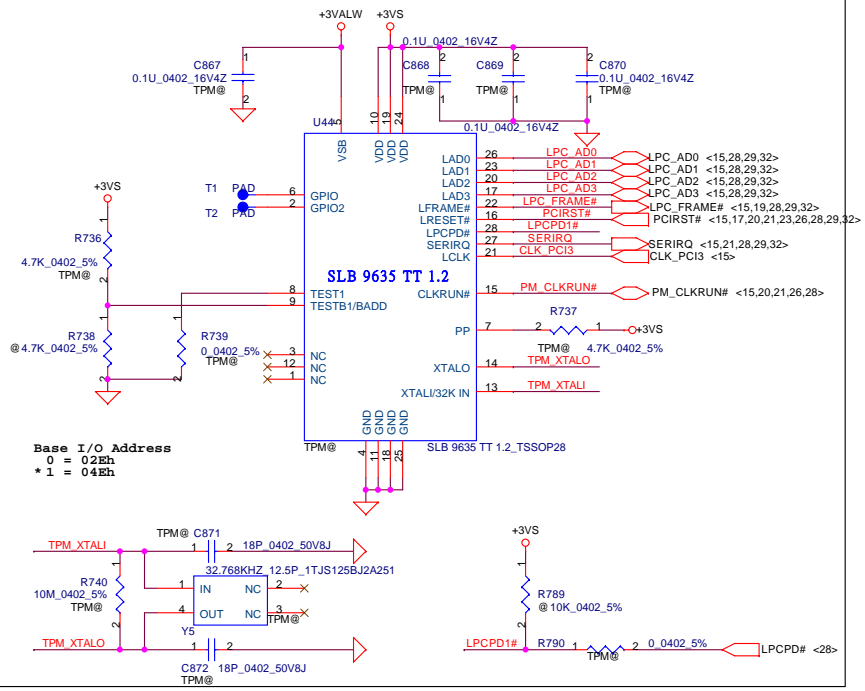
KSI0[.7]	KSI[0..7]	<28,30>
KSO[0..15]	KSO[0..15]	<28>

INT_KBD CONN.

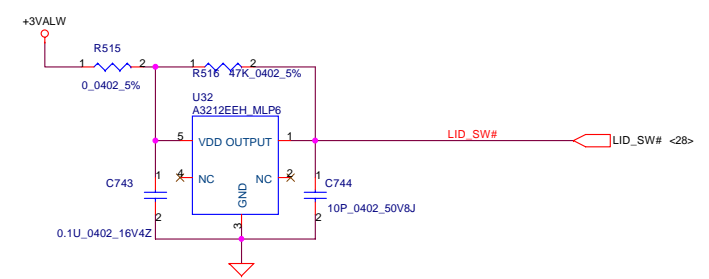


KSO7	C241	100P_0402_25V8K	KSO15	C250	100P_0402_25V8K
KSO6	C236	100P_0402_25V8K	KSO14	C249	100P_0402_25V8K
KSO5	C235	100P_0402_25V8K	KSO13	C244	100P_0402_25V8K
KSO4	C227	100P_0402_25V8K	KSO12	C240	100P_0402_25V8K
KSO3	C242	100P_0402_25V8K	KSO10	C233	100P_0402_25V8K
KSI4	C239	100P_0402_25V8K	KSO11	C247	100P_0402_25V8K
KSI2	C228	100P_0402_25V8K	KSO10	C248	100P_0402_25V8K
KSO1	C231	100P_0402_25V8K	KSI1	C230	100P_0402_25V8K
KSO0	C232	100P_0402_25V8K	KSI2	C229	100P_0402_25V8K
KSI5	C237	100P_0402_25V8K	KSO9	C245	100P_0402_25V8K
KSI6	C238	100P_0402_25V8K	KSI3	C234	100P_0402_25V8K
KSI7	C243	100P_0402_25V8K	PADS_LED#	C252	100P_0402_25V8K
KSO8	C246	100P_0402_25V8K	NUM_LED#	C253	100P_0402_25V8K
			CAPS_LED#	C251	100P_0402_25V8K

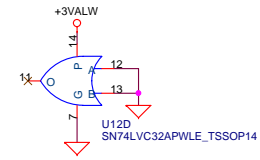
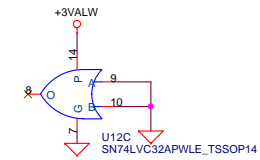
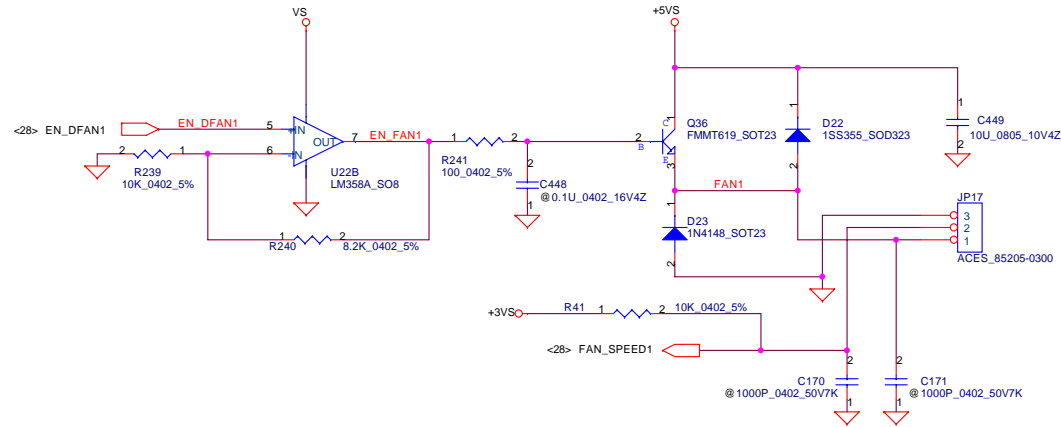
TPM1.2 on board



Lid Switch

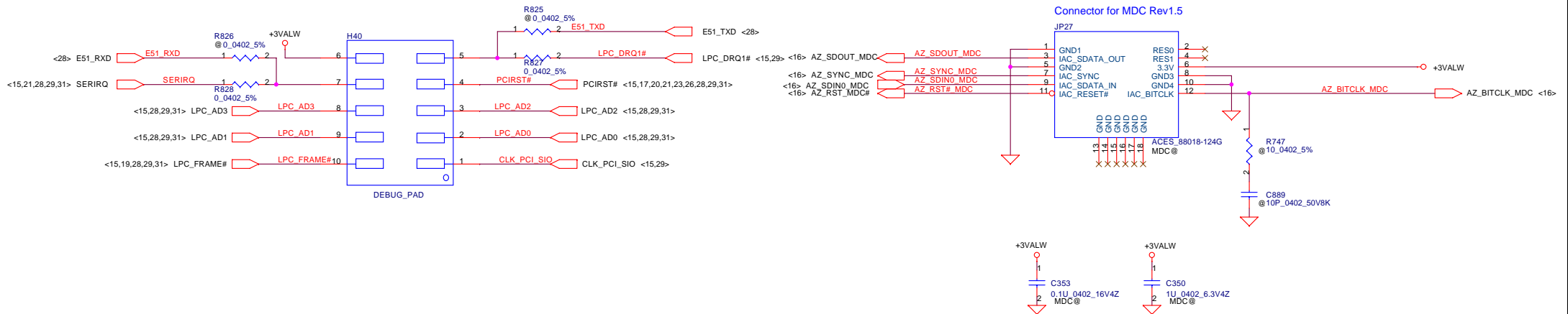


FAN



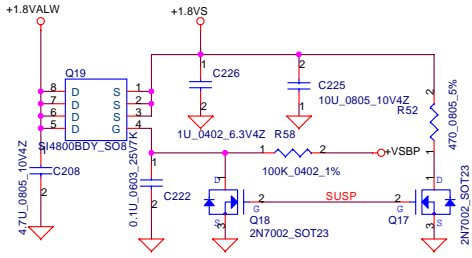
MDC CONN.

Connector for MDC Rev1.5

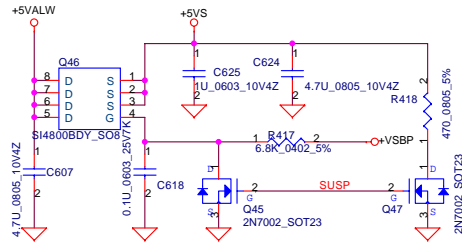


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Date:	Thursday, January 26, 2006	Sheet	32 of 43	Rev 0.3

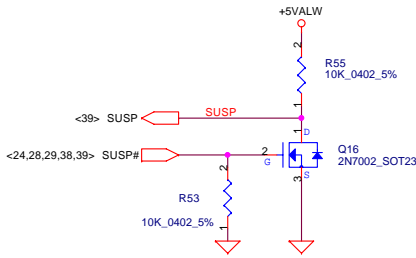
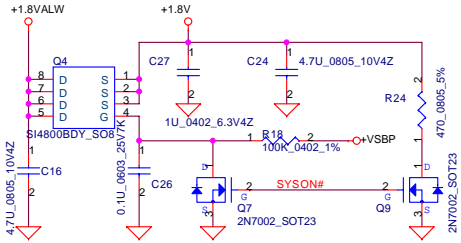
+1.8VALW TO +1.8VS



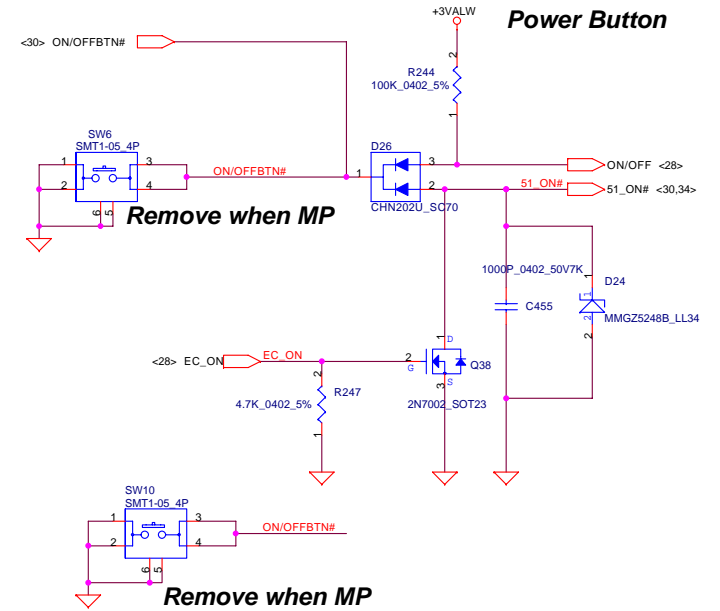
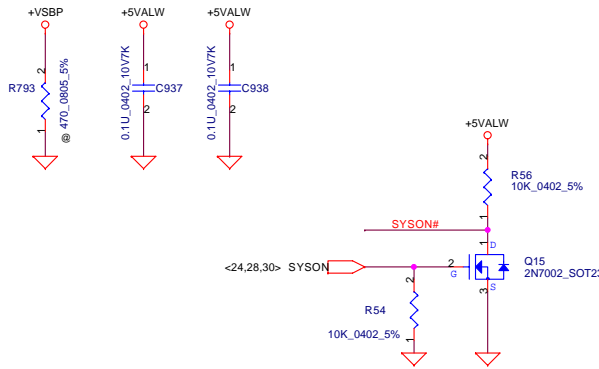
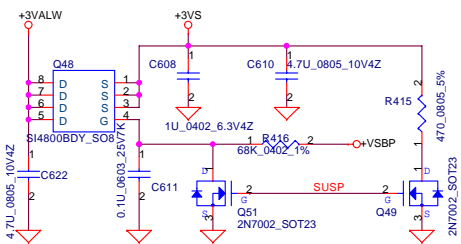
+5VALW TO +5VS



+1.8VALW TO +1.8V



+3VALW TO +3VS



Remove when MP

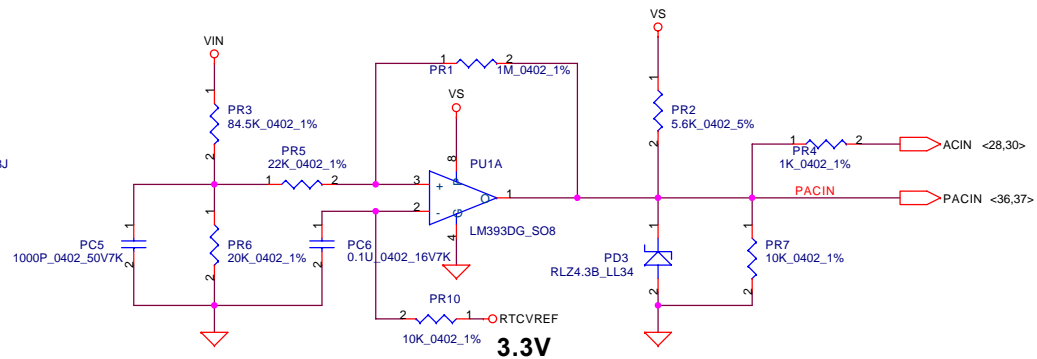
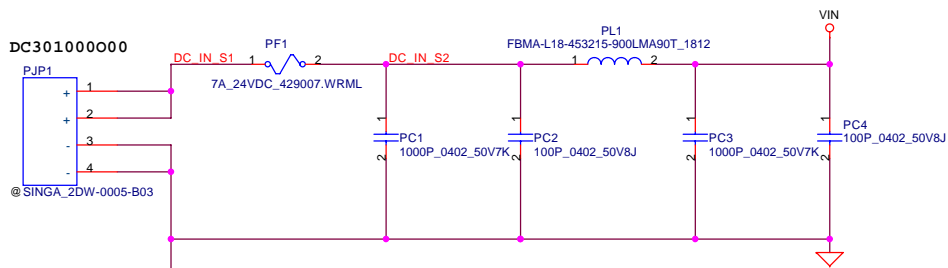
Remove when MP

Compal Electronics, Inc.

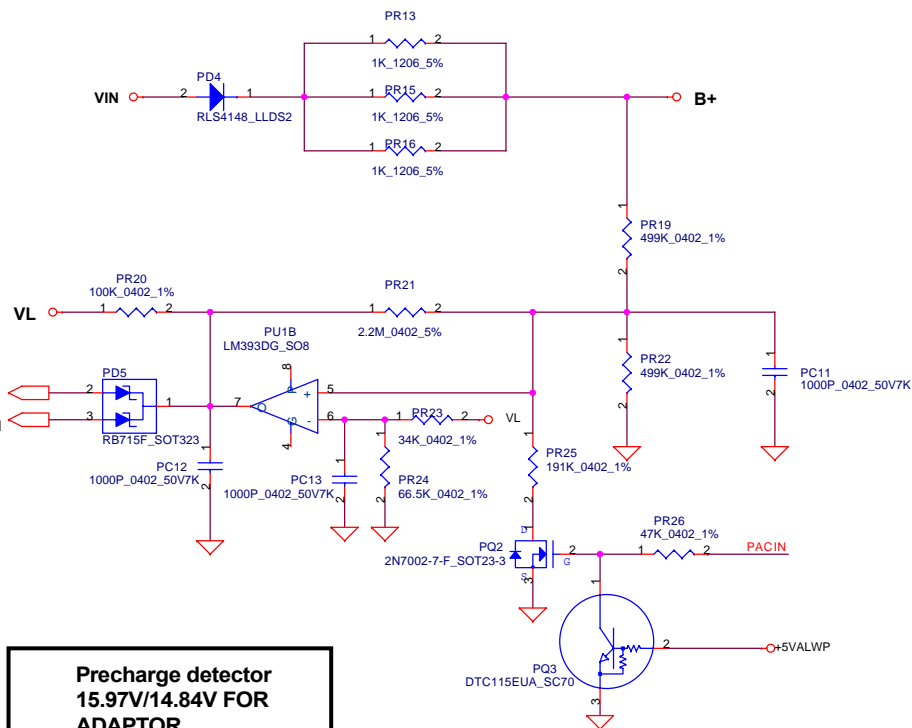
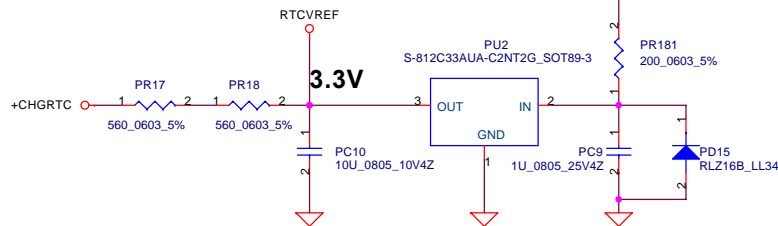
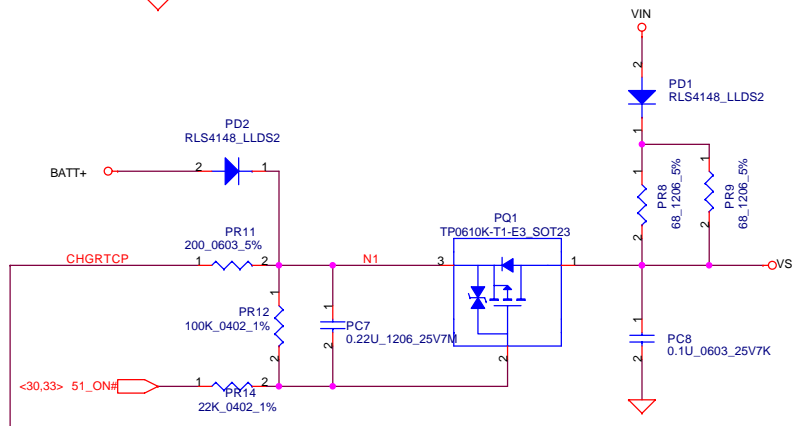
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Title	DC-DC INTERFACE	
Size	Document Number	R ev
	Cust:brHAWAA(LA3141)	0.3
Date:	Thursday, January 26, 2006	Sheet 33 of 43

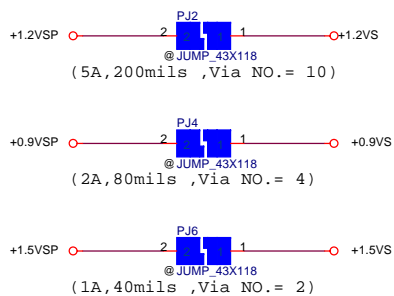
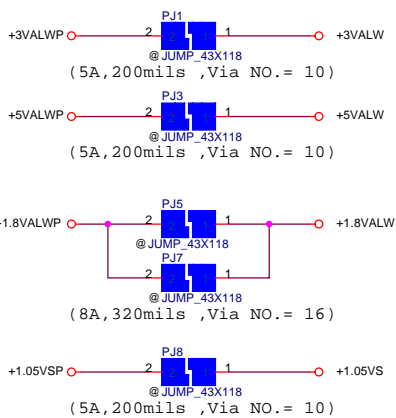
hexain@hotmail.com



Vin Detector
 High 18.384 17.901 17.430
 Low 17.728 17.257 16.976

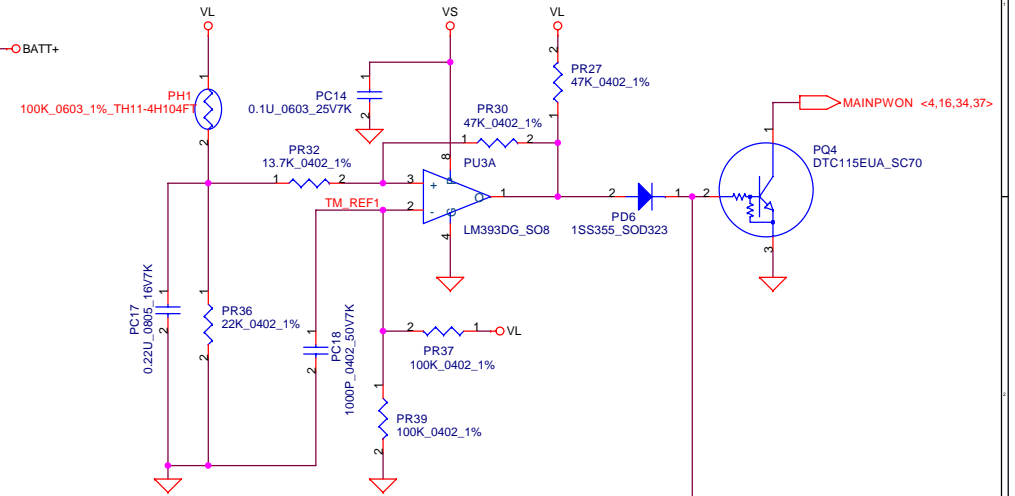
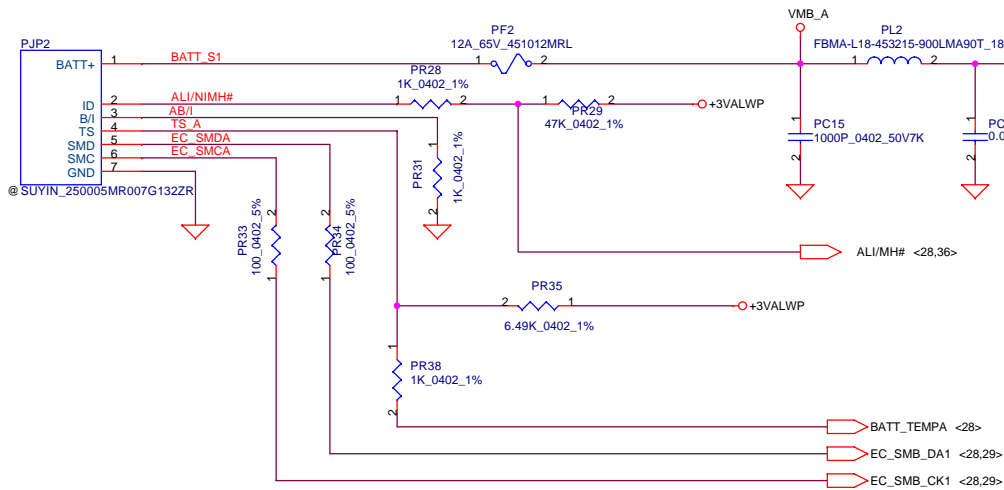


Precharge detector
 15.97V/14.84V FOR
 ADAPTOR

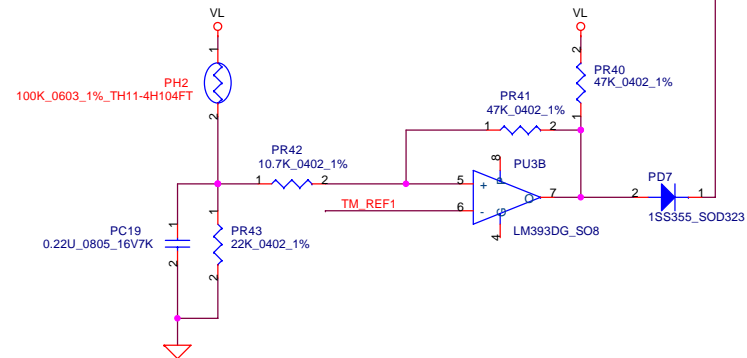
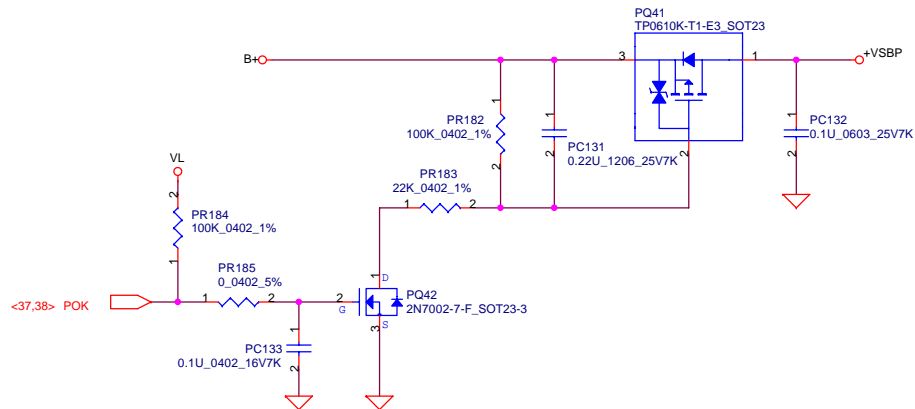


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Date: Thursday, January 26, 2006				Sheet	34 of 43

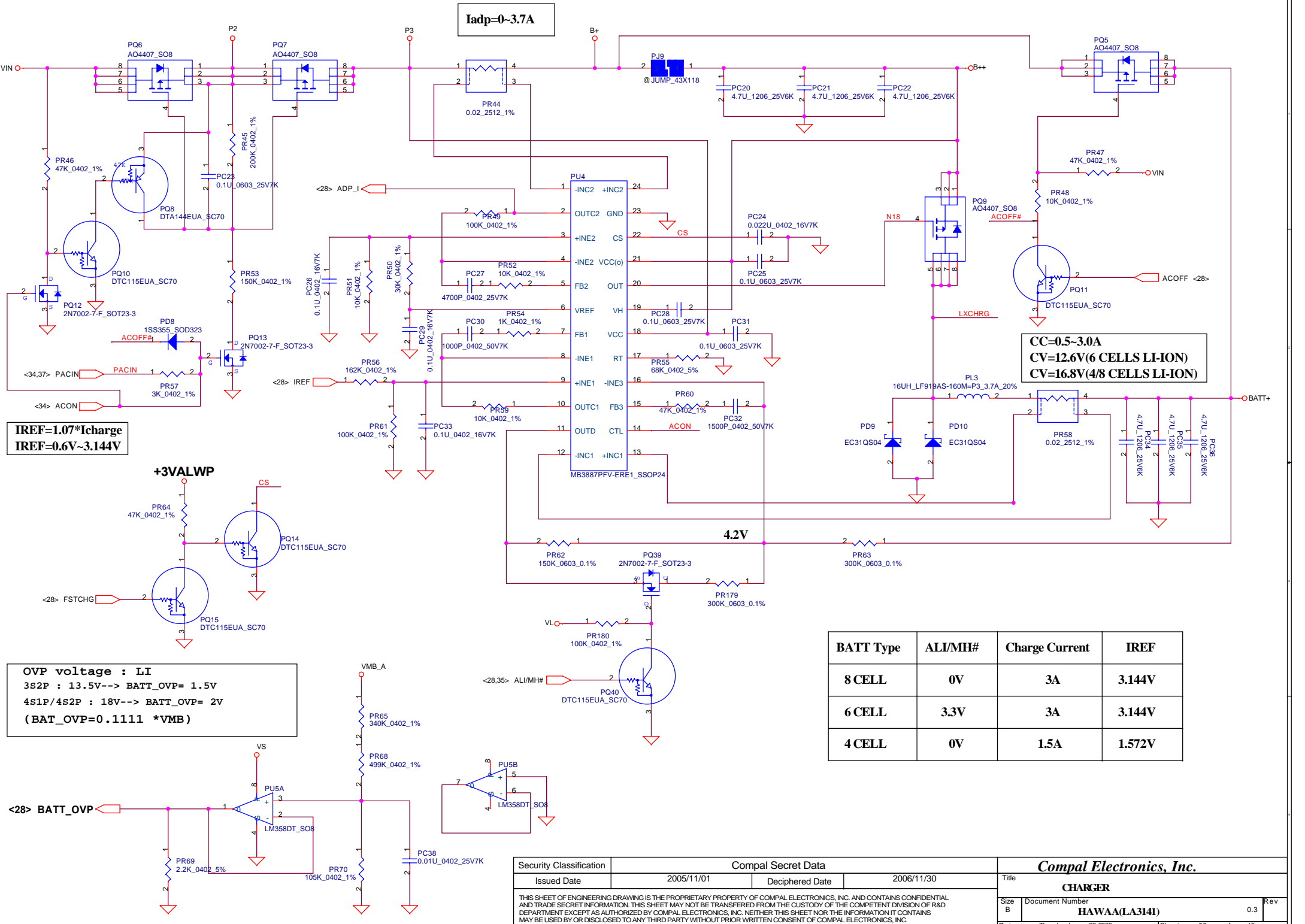
PH1 under CPU botten side :
 CPU thermal protection at 84 degree C
 Recovery at 45 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 45 degree C



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Size	B	Document Number	HAWAA(LA314)	Rev
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I_{adp}=0-3.7A

I_{REF}=1.07*I_{charge}
I_{REF}=0.6V~3.144V

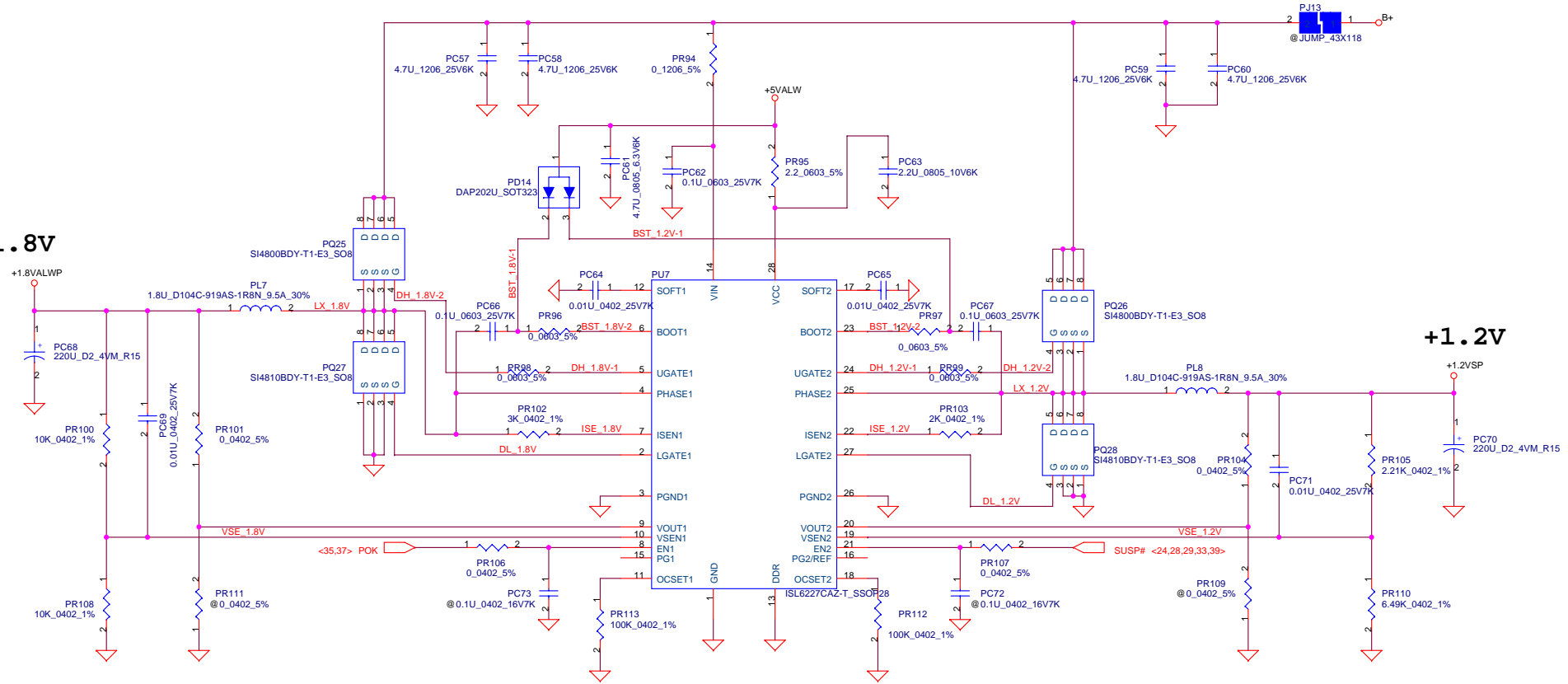
OVP voltage : LI
3S2P : 13.5V--> BATT_OVP = 1.5V
4S1P/4S2P : 18V--> BATT_OVP = 2V
(BATT_OVP=0.1111 *V_{MB})

CC=0.5-3.0A
CV=12.6V(6 CELLS LI-ION)
CV=16.8V(4/8 CELLS LI-ION)

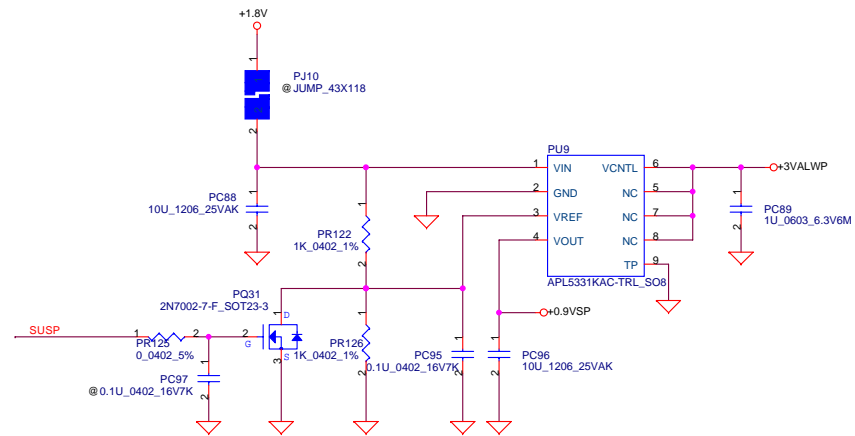
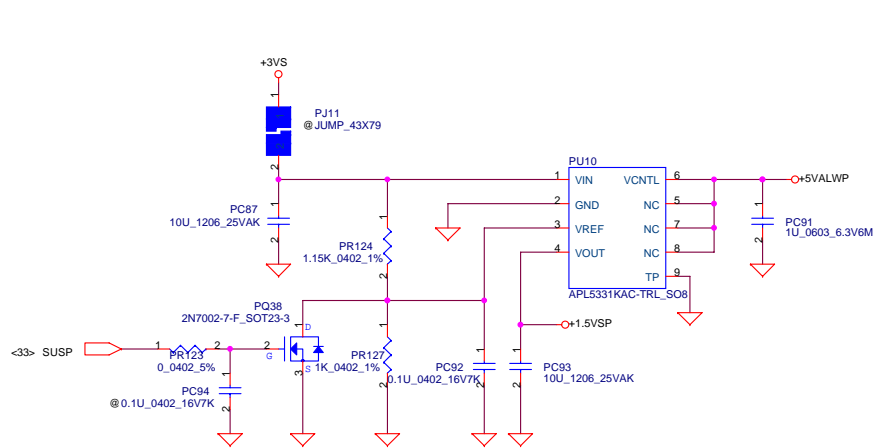
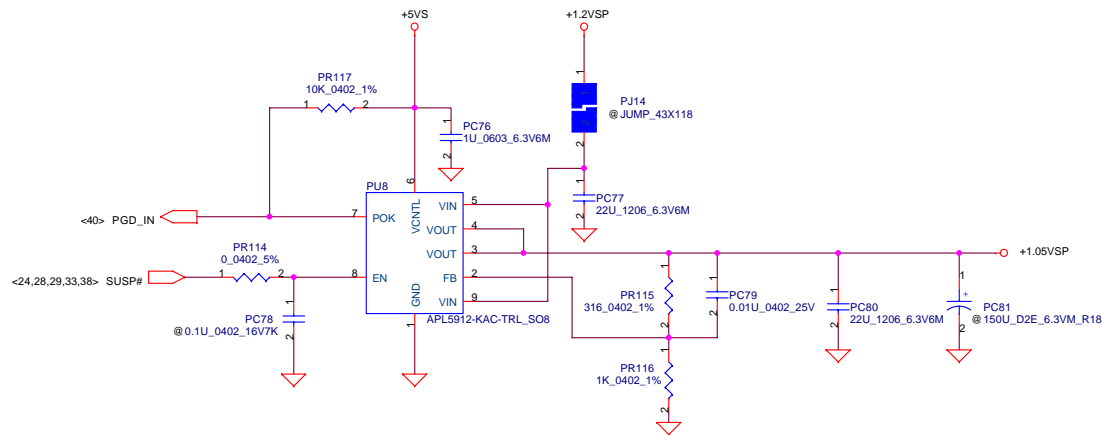
BATT Type	ALI/MH#	Charge Current	IREF
8 CELL	0V	3A	3.144V
6 CELL	3.3V	3A	3.144V
4 CELL	0V	1.5A	1.572V

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Size	B	Document Number	HAWAA(LA314)		Rev	0.3
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+1.8V

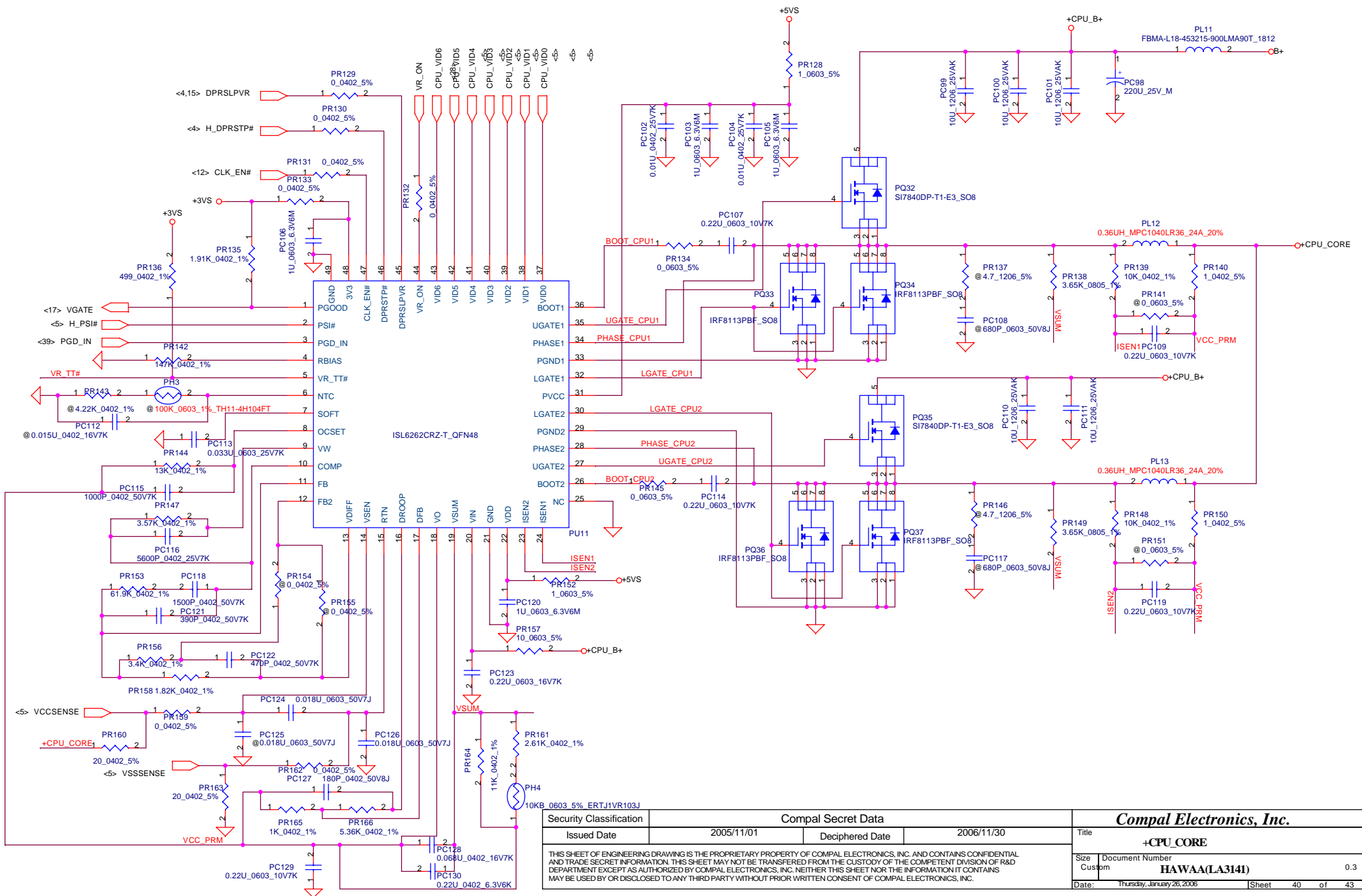


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				Document Number	HAWAA(LA3141)
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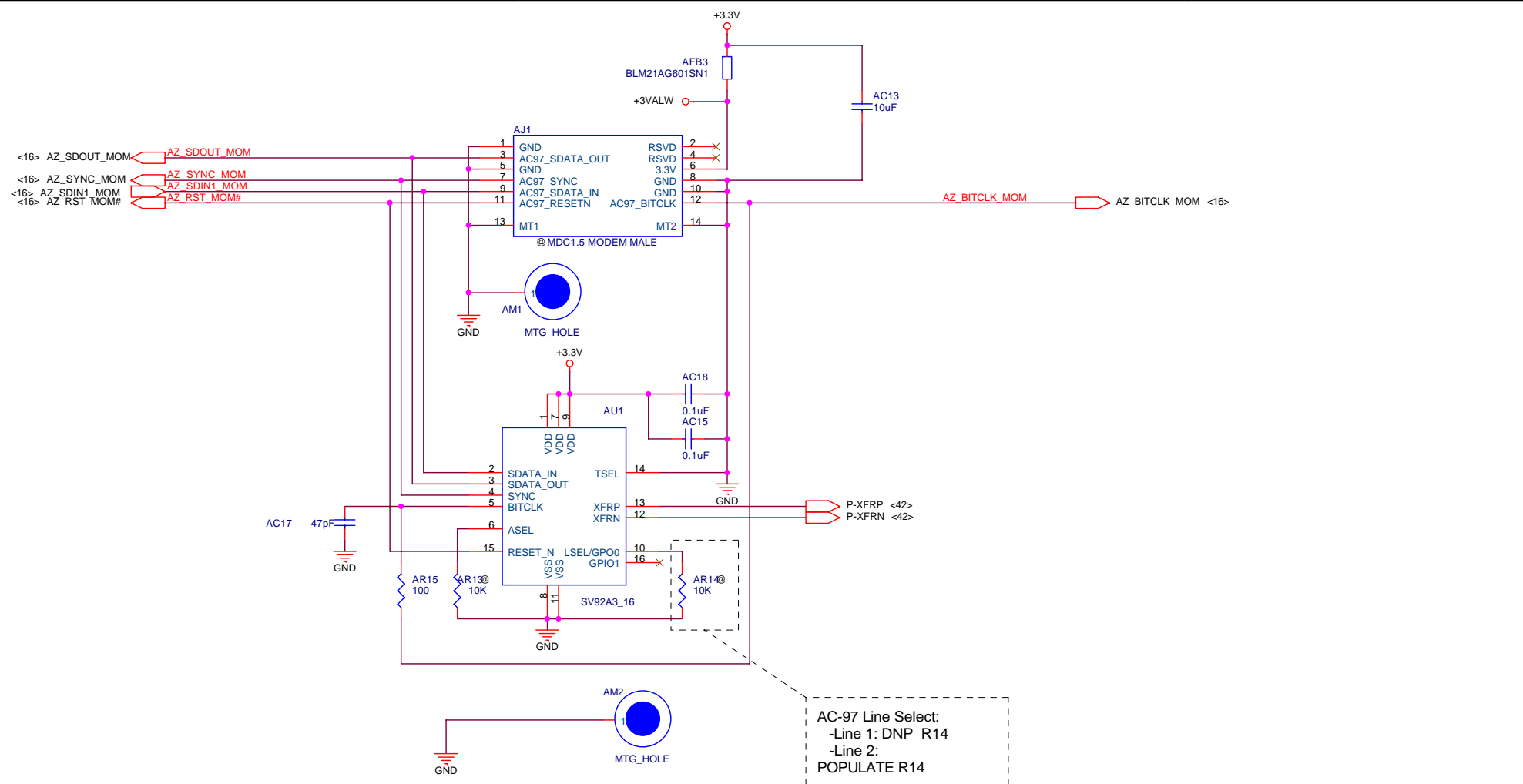


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				+1.05V/+1.5V/+0.9V
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hexrain@hotmail.com



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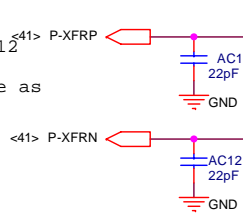


AC-97 Line Select:
 -Line 1: DNP R14
 -Line 2:
 POPULATE R14

Compal Electronics, Inc.		agere systems
123		
Design Engineer: C. Russo		
Title		
DELPHI SV92A3 MDC 1.5 Reference Design		
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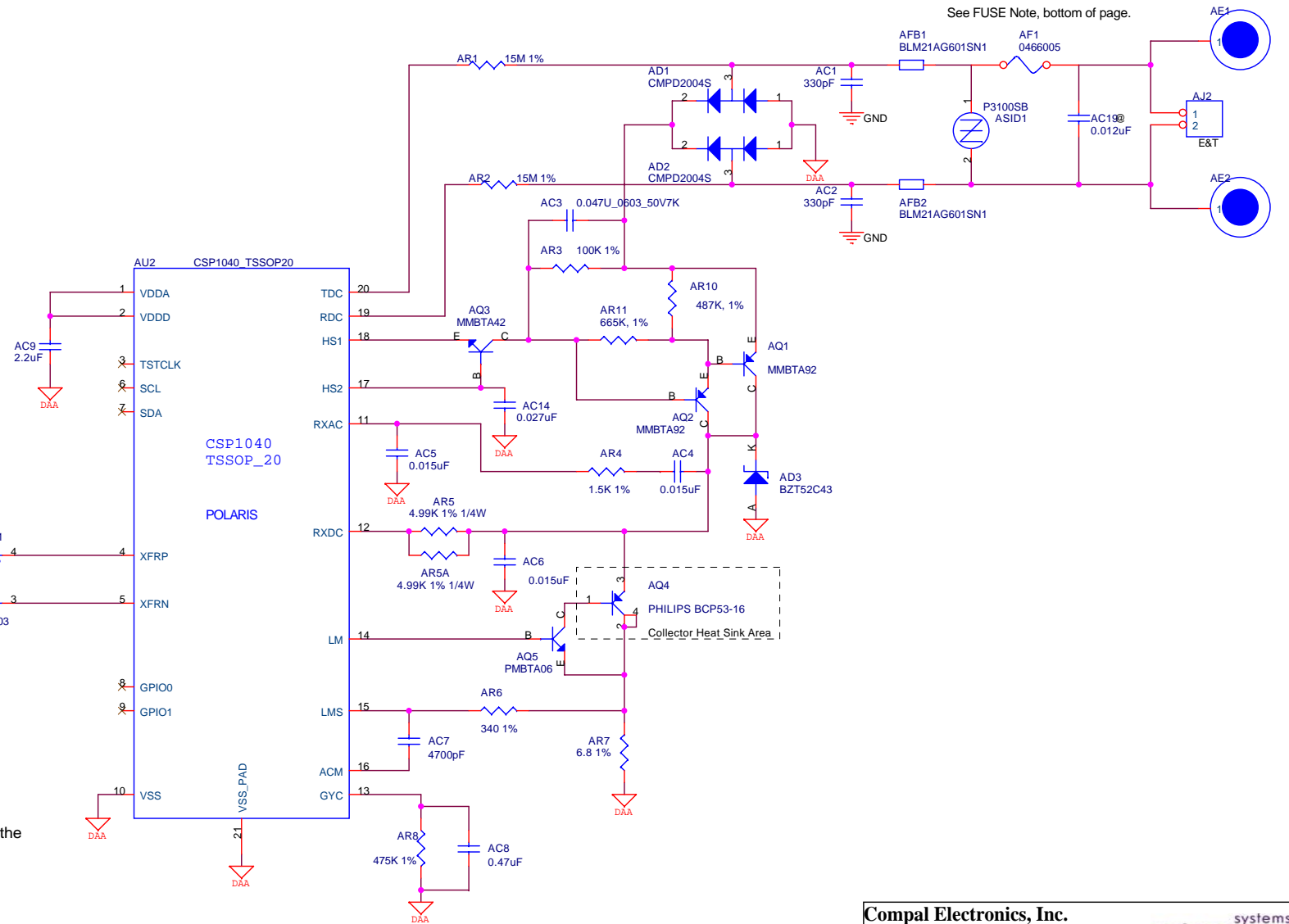
hexainf@hotmail.com

Locate C11, C12^{<41>} P-XFRP as close to digital device as possible.



FUSE Note:
The UL standard UL 1950 dictates the use of a fuse (needed to pass the M1, 600 V, 40A, 1.5 sec) to prevent component flaming during the overvoltage test. Unless one can insure that the modem is in a fire enclosure and provide 26 gauge line cord (acts as a fuse), a fusing element would be required.

Alternatively, if a TNV-1 flame resistant material is used, either as a wrap or cover over the DAA portion of the modem, this could satisfy both overvoltage protection and the separation requirement also contained in UL 1950. This latter requirement provides isolation such that unearthed parts of the DAA cannot be touched by a test finger or test probe.



See FUSE Note, bottom of page.

Compal Electronics, Inc.		agere systems
123		
Design Engineer: R. Trevino		
Title DELPHI SV92A3 MDC 1.5 Reference Design		
Size B	Document Number HAWAA(LA3141)	Rev 0.3
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